25th Anniversary Article: Microstructure Dependent Bias Stability of Organic Transistors

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Recent studies of the bias-stress-driven electrical instability of organic field-effect transistors (OFETs) are reviewed. OFETs are operated under continuous gate and source/drain biases and these bias stresses degrade device performance. The principles underlying this bias instability are discussed, particularly the mechanisms of charge trapping. There are three main charge-trapping sites: the semiconductor, the dielectric, and the semiconductor-dielectric interface. The charge-trapping phenomena in these three regions are analyzed with special attention to the microstructural dependence of bias instability. Finally, possibilities for future research in this field are presented. This critical review aims to enhance our insight into bias-stress-induced charge trapping in OFETs with the aim of minimizing operational instability.

1. Introduction

Organic field-effect transistors (OFETs) have received much attention as switching elements for flexible displays on plastic and their electrical properties are now comparable to those of hydrogenated amorphous silicon (a-Si:H) FETs.[1–9] However, the stability of OFETs is a critical issue that must be addressed before their commercialization.[10–13] First, long-term environmental stability is a prerequisite because displays need operating times greater than several hundred thousand hours. Although OFETs may find a new market in disposable displays, the environmental stability of OFETs remains problematic. Organic semiconductors are used as the active layers of OFETs, but their stabilities are inadequate, so new designs and methods of synthesis need to be developed. Further, the ionization potential of the organic semiconductor should be sufficiently high to guarantee oxidative stability.[14–16] For n-type semiconductors, the lowest unoccupied molecular orbital (LUMO) energy level is more important to stability than the ionization potential.[17–19] The LUMO energy level is also important to the injection barrier to charge carriers from source/drain (S/D) electrodes. For instance, if the ionization potential (>5.5 eV) of a p-type organic semiconductor is too high, hole injection is triggered from the common metal electrode or the conducting polymer; for instance, poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) has a work function of ~5 eV.[1,20] For n-type organic semiconductors, the LUMO energy level needs to match the work function of the S/D electrodes because electron injection occurs from the electrode to the LUMO energy level. To enhance the environmental stability of OFETs, passivation has commonly been used to protect the active layer from atmospheric water and oxygen molecules because they can permeate the active layer. However, most research effort has focused on the development of materials with a high field-effect mobility and good environmental stability.

Another important category of stability is bias-stress stability. FETs operate under continuous gate and S/D biases and these bias stresses can influence device performance.[10] In particular, the threshold voltage shifts (and the on-current changes) upon prolonged gate bias, which will disrupt the functioning of the display pixels connected to the OFET. For example, the brightness of an organic light emitting diode (OLED) driven by an OFET will vary with time because of the continuous gate bias of the OFET. This variation arises because the on-current varies with time in the presence of prolonged gate bias. Further, a liquid crystal display (LCD) driven by an OFET might not turn on/off appropriately when the threshold voltage shift exceeds the operating voltage of the LCD. The general reason for bias instability is charge trapping; the distinctive features of bias-stress effects are discussed further in Section 2. OFETs are layered structures consisting of a semiconductor, a dielectric, a gate electrode, and source/drain electrodes, so each layer as well as the interfaces between the layers (i.e., the semiconductor-dielectric interface, and the semiconductor-source/drain electrodes interface) plays an important role in bias-stress stability. The semiconductor, dielectric, and semiconductor/dielectric interface are the most vulnerable sites for charge trapping. In Section 3, the charge-trapping phenomena in these three regions are discussed with special attention to the dependence of the bias stability of OFETs on their microstructures.

Because microstructural defects themselves or/and their connection with extrinsic factors (i.e., atmospheric molecules)

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serve as trapping sites, minutely microstructural control of these defects is important for achieving high bias-stability and the related representative works will be introduced. In the final section of this review, we suggest some guidelines for future research in this field.

2. Bias-stability Effect of Organic Transistors

In the first study of bias-stress effects on organic transistors in 1999, Matters et al. observed a reversible threshold voltage shift in polythienylene vinylene transistors under a constant negative gate bias.[21] After a prolonged period under a defined continuous or alternating voltage applied to its source, drain, and gate electrodes, an organic transistor commonly exhibits bias-stress effects, such as an increase in the sub-threshold voltage, a reduction/enhancement in the field-effect mobility, an increase in the OFF current, and/or a shift in the threshold voltage. In many systems, the typical bias-stress effect is a shift in the threshold voltage in the direction of the applied gate-bias stress, that is, towards more negative or positive values for an applied negative or positive gate voltage respectively.

A general method for the study of bias-stress effects on organic transistors is to measure the variation in their transfer characteristics over time. A constant gate voltage is applied to the organic transistor; to determine the changes in the transfer curves, the applied gate voltage is interrupted at short time intervals by a sweep of the gate voltage (**Figures 1**a,b). This method has the advantage of determining not only the shift in the threshold voltage but also the changes in the field-effect mobility, sub-threshold swing, and OFF current. However, the proportion of trapped charges can be immediately recovered during the time intervals for a sweep of the gate voltage. Another method is to measure the drain current as a function of time. Constant drain and gate voltages are applied with a linear regime ($|V_D| << |V_G|$) over a period of time (Figure 1c). This method is better than the determination of the changes in transfer curves because there is no recovered charges during the measurement. However, it is only applicable to "ON-state" bias stress and the field-effect mobility must be assumed to be constant for quantitative analysis.

A number of models have been suggested for the quantitative analysis of threshold voltage shifts. Above all, most researchers benchmark the models describing the bias-stress effect in a-Si:H transistors.[22–27] The threshold voltage shift is basically related to the density of trapped charges, N_{tr} : $\Delta V_{th}(t) = eN_{tr}(t)/C_{GD}$, where C_{GD} is the capacitance of the gate dielectric. In addition, the dependence of the charge-trapping rate on the free-carrier density N_f is assumed to be given by diffusion theory:

$$\frac{dV_{th}}{dt} \propto \frac{dN_{tr}}{dt} \propto N_f(t)^{\alpha} \frac{t^{\beta-1}}{\tau^{\beta}} \quad (1)$$

$$\tau = \omega^{-1}\exp\left(E_A / k_B T\right) \quad \beta = T/T_0 \quad (0 \le \beta \le 1) \quad (2)$$

where τ is the characteristic time, β is the dispersion parameter, ω is the attempt-to-escape frequency, E_A is the activation energy, and $k_B T_0$ is the characteristic energy.

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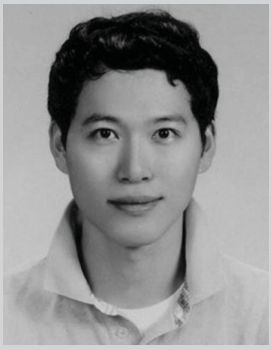

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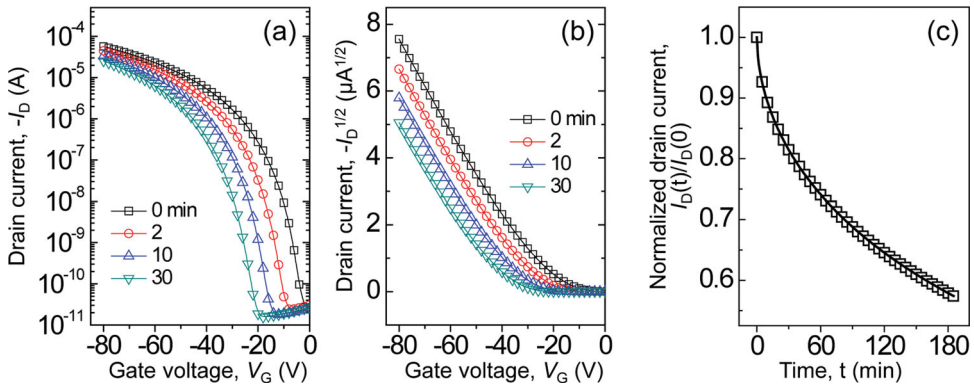

Figure 1. (a,b) Typical transfer curves of pentacene transistors subjected to a prolonged period of gate-bias stress ($V_G = -80$ V). The threshold voltage can be defined as the extrapolation of the linear part of the transfer curves to the gate voltage axis. (c) In situ measurements of the drain current of a pentacene transistor as a function of the bias-stress time for a fixed $V_G = -60$ V, $V_D = -5$ V.

It has been proposed that bias-stress-induced charge trapping consists of two steps: 1) finding and 2) trapping.[28] Firstly, the finding step is the process through which the mobile carriers arrive at a deep trap site. Hence, the frequency of encounter between a mobile carrier and deep trap sites is likely to be dependent on the density of trap sites and on the diffusivity of mobile carriers, which can be represented as an attempt-to-escape frequency ω.[23,27] The characteristic time τ of this process is typically understood as the mean time that charge carriers are in the mobile state. τ decreases as the probability of encounters between mobile charge carriers and trap sites increases. This probability is closely related to the attempt-to-escape frequency ω. For example, a recent result has shown that polymer chain-ends exposed at the semiconductor/gate-dielectric interface act as charge trap sites under bias stress and that ω increases with their density.[29] Secondly, the trapping step is the process of trapping mobile carriers that are near trap sites; this process will have an energy barrier. E_A and k_BT_0 are the mean value of the barrier height and the width of the barrier distribution respectively, but their exact meanings are still elusive.[30,31] It has been proposed that metastable deep trap sites are generated by gate bias, and that E_A and k_BT_0 are related to the activation energy of creating charge-trapping sites.[31,32] Then E_A commonly depends on the chemical structures of the organic semiconductor and the gate dielectric, and of the interface between the two layers. For example, Miyadera et al. found that a pentacene FET with β-PhTS-treated SiO_2 has a higher E_A than one with untreated SiO_2, and thus has a different bias-stress stability.[30] Park et al. also found that the number of fluorine atoms bonded to organic semiconductor molecules affects E_A.[33] A large value of k_BT_0 corresponds to a wider distribution of energy barriers and results in a fast shift in the threshold voltage during the early stages of bias stress.[34]

The solutions of Equation (1) describe the threshold voltage shift with the following stretched-exponential and stretched-hyperbola formulas:[31,35,36]

$$\Delta V_{th}(t) = [V_G - V_{th}(0)] \cdot \left[1 - \exp\left\{-\frac{t}{\tau}\right\}^{\beta}\right] \quad \text{when} \quad \alpha = 1 \tag{3}$$

$$\Delta V_{th}(t) = [V_G - V_{th}(0)] \cdot \left[1 - \left\{\exp\left(\frac{k_BT \cdot \ln(\omega t) - E_A}{k_BT_0}\right) + 1\right\}^{\frac{1}{1-\alpha}}\right]$$

$$\text{when} \quad \alpha > 1 \tag{4}$$

As shown in Equations (3) and (4), the solutions depend strongly on the value of the stretching factor α, whose meaning is still unclear. α will be unity only if the diffusion mechanism is defined properly. In this case, Equation (3) is typically used. However, several authors have reported deviations from Equation (3), in particular for long stress times ($t > 10^4$ s) and wide temperature ranges. To account for this behavior, $\alpha > 1$ has to be introduced into Equation (1), which yields the stretched hyperbola formula in Equation (4). Experimentally, one can, of course, obtain four fitting parameters (ω, E_A, k_BT_0, and α) from a single bias-stress experiment. However, the accuracy of these values decreases as the number of fitting parameters increases. Hence, a number of researchers have used Equation (4) by assuming values for ω and α of 10^5 Hz and 1.5 respectively and then tried to extract accurate values for E_A and k_BT_0.[37] If the FET mobilities are constant under bias stress, Equations (3) and (4) can be converted into functions of drain current (I_D):

$$I_D(t) = t_D(0) \cdot \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] \quad \text{when} \quad \alpha = 1 \text{ and } |V_D| \ll |V_G| \tag{5}$$

$$I_D(t) = t_D(0) \cdot \left[1 - \left\{\exp\left(\frac{k_BT \cdot \ln(\omega t) - E_A}{k_BT_0}\right) + 1\right\}^{\frac{1}{1-\alpha}}\right]$$

$$\text{when} \quad \alpha = 1 \text{ and } |V_D| \ll |V_G| \tag{6}$$

Values for various OFETs of τ, β, ω, and E_A obtained by fitting the threshold voltage shifts with Equations (3) or (4) are presented in **Table 1**. τ is the preferred parameter for the quantitative description of bias-stress stability. For instance, it depends on E_A according to Equation (2), so slight changes in E_A result in significant changes in τ. As shown in Table 1, most

Table 1. Characteristic times (τ), dispersion parameters (β), attempt-to-escape frequencies (ω), activation energies (E_A) of various kinds of organic transistors at room temperature, obtained with Equations (3) or (4). * These parameters were extracted from Equation (4), and ω and α were assumed to be 10^5 Hz and 1.5 respectively to minimize the fitting error for E_A and β.

Semiconductor	Gate-dielectric	τ [s]	ω [Hz]	E_A [eV]	β	Reference
PTAA	HMDS-SiO_2	1×10^7	10^3	0.6 ± 0.1	0.30	[11]
Pentacene	bare SiO_2	$1.4 - 3.3 \times 10^2$	–	0.08–0.09	0.31–0.35	[30]
	β-PhTS-SiO_2	$1.6–6.9 \times 10^6$	–	0.4	0.19	
	BCB-Al_2O_3	2.4×10^5	–	–	0.41	[46]
	HMDS-SiO_2	7.1×10^5	10^5	0.602	0.45	[47]*
	Allyl-SiO_2	4.0×10^5		0.575	0.49	
	Propyl-SiO_2	4.5×10^5		0.578	0.49	
	Chloro-SiO_2	5.9×10^5		0.585	0.48	
	Octyl-SiO_2	1.8×10^5		0.554	0.51	
	ODTS-SiO_2	1.2×10^5		0.544	0.54	
	PS	$3.3–21 \times 10^5$	$10^5–10^6$	0.6	0.55–0.63	[29]
	PI	5.0×10^2	–	–	0.35	[48]
	PMMA	1.2×10^4	–	–	0.45	[49]
Pentacene (single crystal)	ODTS-SiO_2	4.0×10^3	10^8	0.67		
C8-BTBT	bare SiO_2	1.4×10^2	–	–	0.25	[50]
	PVP	2.0×10^1	–	–	0.30	
	PMMA	4.9×10^3	–	–	0.40	
	Cytop	1.3×10^4	–	–	0.22	
P3HT	HMDS-SiO_2	4×10^7	10^3	0.6	–	[11]
	PSSH (electrolyte)	1×10^2	10^{12}	0.82	–	[51]
α-sexithophene	SiO_2	$3.4–5.9 \times 10^3$	–	–	0.5–0.6	[52]
		–	–	0.52	0.79	[31]*
TIPS-PEN (single crystal)	parylene	1.8×10^5	–	–	0.37	[53]
Tetracene (single crystal)		3.1×10^4	–	–	0.37	
Rubrene (single crystal)		5.0×10^7	–	–	0.37	
TES-ADT	ODTS-SiO_2	3.6×10^5	10^5	0.572	5.3	[54]*
	bPS-SiO_2	1.3×10^6	–	0.845	2.86 (bPS1.6k)	
		4.5×10^5		0.638	4.73 (bPS19.5k)	
	PHS	1.0×10^5	10^5	0.54	0.46	[55]*
	PFS	4.9×10^6		0.70	0.37	
8–3-NTCDI	HMDS-SiO_2	2.8×10^4	–	–	0.56 (air) 0.31 (N_2)	[56]
		7.7×10^6				
	ODTS-SiO_2	1.2×10^4	–	–	0.59 (air) 0.32 (N_2)	
		2.9×10^5				

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Table 1. Continued.

Semiconductor	Gate-dielectric	τ [s]	ω [Hz]	E_A [eV]	β	Reference
MonoF-IF-dione	PS	9.3×10^2	10^5	0.477	0.79	[33]*
TriF-IF-dione		3.2×10^5		0.629	0.57	
PDI-8	SiO_2	7.5×10^3	–	–	0.32	[57]
PDI-8CN_2		3.9×10^4	–	–	0.41	
PQTBTz-C12	ODTS-SiO_2	5×10^7	–	–	0.2–0.3	[58]
F8T2	SiO_2	1.5×10^4	–	0.52	–	[38]
a-Si		8×10^7	10^9	0.98		[37]
μc-Si		10^{12}	10^6	1.07		[59]

Organic semiconductor
- PTAA: polytriarylamine
- C8-BTBT: dioctylbenzothienobenzothiophene
- P3HT: poly 3-(hexylthiophene)
- TIPS-PEN: 6,13-Bis(triisopropylsilylethynyl)pentacene
- TES-ADT: 5,11-bis(triethylsilylethynyl) anthradithiophene
- 8–3-NTCDI: *N*,*N*′-bis(3-(perfluorocotyl)propyl)-1,4,5,8-naphthane tetracarboxylic diimide
- MonoF-IF-dione: fluoro-benzene-sustituted indenofluorenediones
- TriF-IF-dione: trifluoro-benzene-substituted indenofluorenediones
- PDI-8: *N*,*N*′-bis(*n*-octyl)-perylene-3,4:9,10-bis(dicarboximide)
- PDI-8CN_2: *N*,*N*′-bis(*n*-octyl)-1,6-dicyanoperylene-3,4:9,10-bias(dicarboximide)
- PQTBTz-C12: poly(didodecylquarterthiphene-*alt*-didodecylbithiazole)
- F8T2: poly(9,9- dioctylfluorene-*alt*-bithiophene)

Gate-dielectric
- HMDS-SiO_2: hexamethyldisilazane-treated SiO_2
- *β*-PhTS-SiO_2: β-phenethyltrichlorosilane-treated SiO_2
- BCB: divinyltetramethyldisilozane-bias(benzocyclobutene)
- Allyl-SiO_2: allyltrichlorosilane-treated SiO_2
- Propyl-SiO_2: *n*-propyltrichlorosilane-treated SiO_2
- Chloro-SiO_2: 3-chloropropyltrichlorosilane-treated SiO_2
- Octyl-SiO_2: *n*-octyltrichlorosilane-treated SiO_2
- ODTS-SiO_2: *n*-octadecyltrichlorosilane-treated SiO_2
- PS: polystyrene
- PI: polyimide
- PMMA: polymethylmetacrylate
- PSSH: poly(styrene sulfonic acid) (electrolyte)
- bPS: polystyrene brush
- PHS: cross-linked poly(4-hydroxyl styrene)
- PFS: cross-linked poly(3-(hexafluoro-2-hydroxyl) propyl styrene)

values of E_A are much larger than thermal energies (26 meV), which indicates that the energy barrier to trapping is not easily overcome. Moreover, the chemical and physical structures of the semiconductor and the gate dielectric affect E_A and τ significantly. The following section discusses the relationship between the chemical and physical structures and bias-stress stability in detail. Even though these models can be used to describe typical bias-stress effects in organic transistors, they cannot account for undesirable bias-stress effects such as increases in the drain current because our understanding of the microscopic origins of charge trapping is incomplete. For example, hydrogen diffusion is regarded as the main origin of bias-stress effects in *a*-Si:H transistors and Equation (3) was derived accordingly. If the actual origin of bias-stress effects in OFETs is clarified, a more accurate model of the threshold voltage shift could be developed. Street et al. proposed that the formation of bipolarons in organic semiconductors is one source of bias-stress effects in OFETs,[38–40] and Lee et al. found a bias-stress-induced absorption peak below the π–π* absorption edge, which is considered to be the bipolaron energy level.[41–43] Based on this mechanism in which two free carriers form a bipolaron, a rate equation for the response to bias stress can be derived as follows: $dN_f/dt = -kN_f^2 + bN_{BP}$, where N_{BP} is the bipolaron concentration, and k and b are rate constants. On the other hand, Sharma et al. proposed that proton migration into SiO_2 gate dielectrics is the origin of bias-stress effects and suggested a drift-diffusion model.[44,45] Thus, establishing the actual mechanism of bias-stress-induced charge trapping is a prerequisite for the accurate prediction of the changes in the electrical characteristics under bias stress. In OFETs, bias-stress effects originate from the various types of charge trap sites in the distinct layers and at their interfaces. The actual locations of bias-stress-induced charge traps could be in the organic semiconductor, the gate dielectric, or the interface between the two layers, and the type of predominant charge trap also varies with the material, device architecture, measurement conditions, etc. Various studies have focused on classifying the predominant charge trap sites in these three categories, but research into the effects of nano/microscopic morphology and molecular design on bias-stress stability is still in its infancy. Indeed, to understand the predominant mechanisms of bias-stress effects, we need to determine the general relationship between such effects and the chemical and physical nature of the organic semiconductor, the gate dielectric, and the interface between these two layers.

3. Stability Issues

3.1. Semiconductor

Organic semiconductors have received considerable attention as promising channel materials because of their easy processability and the tunability of their optoelectrical properties for FET applications.[9,60] Nowadays, their charge carrier mobilities and environmental stabilities are comparable to or even better than those of a-Si:H.[14,61] Novel molecular designs, optimization of the nanostructures in thin films, interface engineering in OFET architectures, and the introduction of well-defined passivation layers on top of OFET devices have resulted in

successful applications in commercial display backplanes.[1,2,20] However, on the microscopic scale, OFETs based on organic polycrystalline, semicrystalline or amorphous semiconductors can exhibit more electrical instability under external bias stress than those with single-crystalline nature.[53] This variable instability of organic semiconductors arises because of variation in the numbers and types of charge (hole or electron) traps created in disordered (amorphous) regions, at grain boundaries between crystallites in the channel, or at the interfaces between channels and dielectric components or channels and S/D electrodes.

In this section, we provide a general overview of the charge-trapping sites arising due to defects in the electronic density of states (DOS) and in the disordered regions or grain boundaries in the structures of organic semiconductor thin films. These charge-trapping sites can lead to a detrimental shift in the threshold voltage under gate and S/D bias stress. Such bias-stress instabilities have recently been observed in OFETs for a wide range of p- and n-type organic semiconductors: in vacuum-deposited small molecules to solution-processed polymers, including pentacene, pentacene and oligothiophene derivatives, polytriarylamine (PTAA), polythiophene, polythienylenevinylene (PTV), and other charge-transfer type polymer semiconductors, as listed in Table 1.[11] In this regard, many research groups have attempted to produce highly ordered organic semiconductor thin films with a minimal concentration of charge traps that have a high bias stability comparable to those of a-Si:H FETs.[10]

It has been found that the systematic manipulation of molecular or microstructural features such as the electronic energy level (the HOMO level for p-type semiconductors and the LUMO level for n-type semiconductors) and those of the crystalline microstructure (crystallinity, orientation, grain size, and crystalline perfectness) of organic semiconductors can result in electrical instability under bias stress. Although many studies have aimed at enhancing electrical stability, more insight into the relationship between the molecular design and crystalline microstructures of organic semiconductors and their bias stability is still needed.

3.1.1. Effect of Crystalline Microstructure on Bias Stability

In an attempt to determine the microstructural origin of bias-stress-driven electrical instability in OFETs, many groups have investigated various types of organic semiconductors. The main approach to decreasing the number of charge traps and the intrinsic electrical instability is to enhance the molecular ordering or crystallinity over the whole channel region. In contrast to solution-processed polymer semiconductors, the single-crystalline structures of small molecule semiconductors produced by either vacuum deposition or solution processing typically exhibit high bias stability in OFETs because they contain no grain boundaries or disordered regions. Kalb et al. studied the electrical stability of single-crystalline small molecule organic semiconductors (i.e., pentacene and rubrene) under bias stress, as shown in **Figures 2**a and b.[62] In particular, they found that rubrene single crystal field-effect transistors (SC-FETs) do not exhibit a threshold voltage shift ($\Delta V_{th} < 0.2$ V) during positive (OFF-state) or negative (ON-state) gate bias stress at $V_G = \pm 70$ V for 2 h under an inert atmosphere. In contrast, the bias-stress stabilities of thin films with polycrystalline microstructures and grain boundaries are significantly worse, with a larger negative gate voltage shift of $\Delta V_{th} = 5.2$ V during the application of $V_G = -70$ V for 2 h. This result indicates that the structural defects present in thin films with polycrystalline microstructures have an important influence on charge-trapping characteristics. They concluded that intrinsic structural perfection is required in an organic semiconductor for high electrical stability. The bias-stress stability of n-type SC-FETs based on *N,N′*-bis(n-alkyl)-(1,7 and 1,6)-dicyanoperylene-3,4:9,10-bis(dicarboximide)s (PDIF-CN2) small molecules was also investigated, as shown in Figures 2c and d.[63] Barra et al. found that there was a decrease in the S/D current of the PDIF-CN2 SC-FET of only 1% when $V_G = +80$ V was applied for a week under vacuum, which is as small as that of p-type SC-FETs.[63] In this regard, single-crystalline microstructures are required in organic semiconductors to enhance the bias-stress stability and field-effect mobility of OFETs.

Note that solution-processed polymer semiconductors exhibit various microstructures depending on the type of repeating units and side-chains, the molecular weight, and the annealing process. As shown in **Figure 3**, Street et al. observed that OFETs based on poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophene), PBTTT, exhibit better bias stability than OFETs based on poly(3,3‴-didodecylquaterthiophene), PQT-12, by a factor of 1.5–2, and concluded that this difference is due to the higher crystallinity of the PBTTT thin film.[64] This crystallinity-dependent bias stability of OFETs has also been demonstrated in other polymer semiconductor systems. Kim et al. reported the crystallinity-dependent bias stability of a device based on a low band-gap semiconducting polymer consisting of electron-rich 2,6-di(thienyl)naphthalene units with decyloxy chains (NAPDO) and electron-deficient diketopyrrolopyrrole units with 2-ethylhexyl chains (DPP-EH), as shown in **Figure 4**a.[65] The OFET based on as-spun pNAPDO-DPP-EH has a low carrier mobility, but thermal annealing significantly improved both the bias stability and the carrier mobility. Figures 4b and c show that the bias-stress stability is strongly correlated with the crystallinity of the polymer films, as revealed by the GIXD results in Figure 4d, which shows that high crystallinity in a semicrystalline polymer semiconductor is of great importance for both efficient charge transport and high electrical stability.

The impacts of crystalline orientation and perfection as well as crystallinity on bias-stress stability were investigated in more detail for a specific organic semiconductor. Kim et al. reported a liquid-crystalline polymer that is a good candidate for both high carrier mobility and bias stability.[58] They demonstrated that the donor-acceptor type/liquid crystalline copolymer poly (didodecylquaterthiophene-*alt*-didodecylbithiazole), PQTBTz-C12, exhibits a high field-effect mobility of 0.33 $cm^2/V \cdot s$, good environmental stability, and unprecedented electrical stability under bias stress.[58,66] They assessed the impact on electrical stability of features of the crystalline microstructure such as crystallinity, chain orientation, and crystal perfection, which were controlled by varying the molecular weight and performing thermal annealing. **Figures 5**a–c show that highly crystalline thin films with preferential edge-on orientation and crystal perfection were formed spontaneously after thermal

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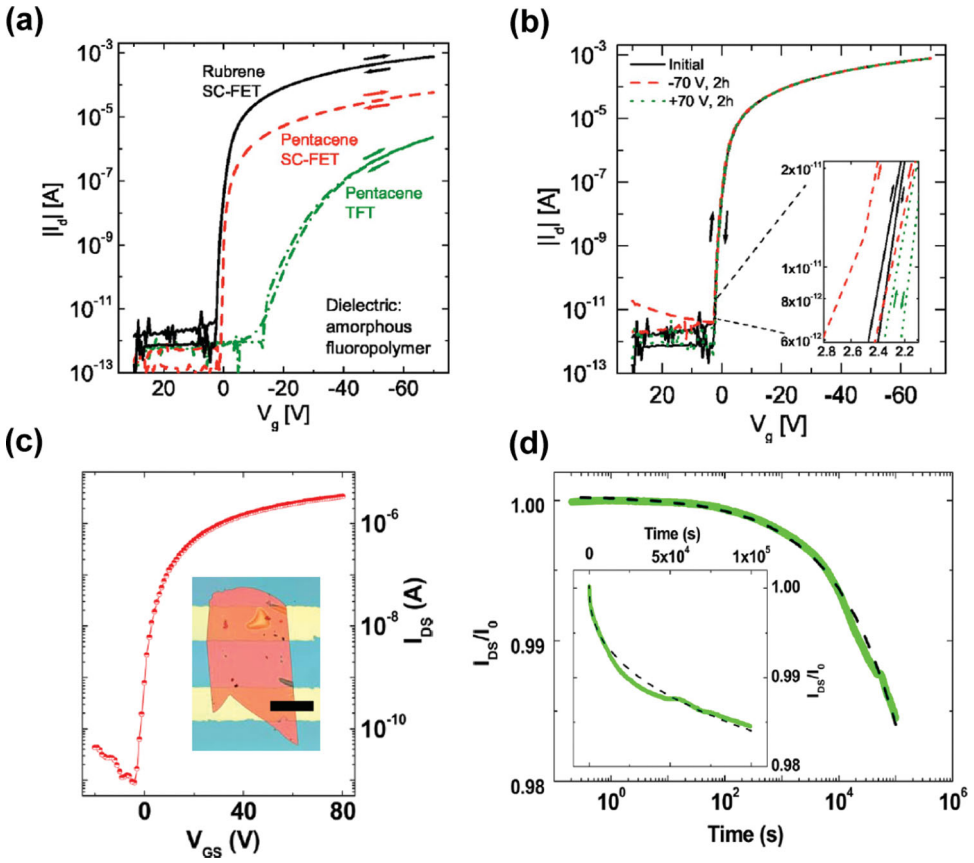

Figure 2. (a) Transfer characteristics measured in the saturation regime of $V_D = -80$ V for a rubrene single crystal (SC)-FET, a pentacene SC-FET, and a pentacene TFT. (b) Bias-stress stability measured at $V_D = -80$ V prior to the stress sequence (full black line), after 2 h of gate bias stress at $V_G = -70$ V (dashed red line), and after subsequent gate bias stress at $V_G = +70$ V for 2 h (dotted green line) for a rubrene SC-FET. The graph includes the forward and reverse sweep in all three cases. The inset shows the drain currents close to the onset voltage. Reproduced with permission from ref [62]. Copyright 2007 American Institute of Physics. (c) Transfer characteristic measured in the linear regime of $V_D = 10$ V for a PDIF-CN2 SC-FET. Inset shows an optical image of a PDIF-CN2 SC-FET. The scale bar is 200 μm. (d) Semi-log plots of the normalized current ($I_D(t)/I_0$) measured in vacuum up to 10^5 s (28 h) while stressing at $V_G = 80$ V ($V_D = 10$ V). Reproduced with permission from ref [63]. Copyright 2012 American Institute of Physics.

annealing through self-organization of individual polymer chains in the liquid-crystalline mesophase. This facilely fabricated highly ordered semiconductor layer with a minimal concentration of charge traps exhibits high electrical stability. The transfer curves shift with stress time in the direction of the applied gate bias, as shown in Figures 5d–f, which could be due to the shallow trapping of charges in less mobile states arising because of microstructural disordering. Further, the subthreshold slope of the device does not change even after the device has undergone gate-bias stressing, which indicates that no additional defect states are created at the channel/insulator interface. Interestingly, it can be seen that the magnitude of the threshold voltage shift decreases with increases in the thermal annealing temperature, from –14.5 V (not annealed) to –2.6 V (annealed at 180 °C). In other words, the device annealed at 180 °C (mesophase) exhibits the lowest threshold voltage shift (the highest electrical stability), which indicates that highly ordered films tend to have enhanced bias stability due to their smaller number of trapping sites.

They also found that depending on the MW (from 13 to 41 kDa) PQTBTz-C12 adopts two different crystalline phases, a liquid-crystalline phase (13, 22 kDa) or a semi-crystalline phase (41 kDa), which have different molecular orderings and nanomorphologies in thin films.[67] These differences result in a change in the bias stability by more than a factor of 3. In **Figure 6**a, the device with 41 kDa semicrystalline PQTBTz-C12 exhibits the highest threshold voltage shift under both ambient and inert conditions, whereas the devices with 13 kDa and 22 kDa liquid-crystalline PQTBTz-C12 exhibit relatively low threshold voltage shifts. Even if all measurements were performed under the same conditions, the threshold voltage shift varied dramatically with the MW of the sample, which implies that a film with more disordered regions can be attacked more easily by water vapor or oxygen. Further, the transfer curves of the 22 kDa device varied little ($\Delta V_{th} = 3 \sim 4$ V) during a period of prolonged bias stress (about 50,000 s) under ambient conditions, as shown in Figure 6b, due to its optimized molecular ordering with fewer defects. Thus charge trapping is minimized at the optimum MW of the PQTBTz-C12 film; at this MW, there are fewer chain end groups and the film is liquid-crystalline in nature. These properties lead to a better bias stability in the polymer semiconductor based OFET.

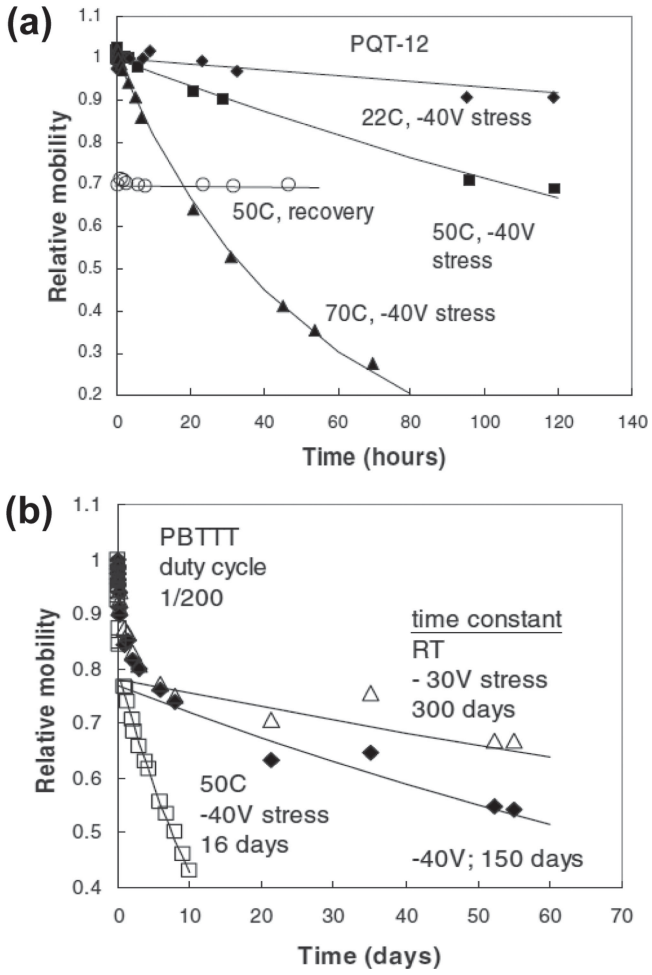

Figure 3. Time dependence of the effective FET mobility for (a) PQT FETs and (b) PBTTT FETs at V_G = −40 V measured at RT, 50 °C, and 70 °C. Reproduced with permission from ref [64]. Copyright 2008 American Physical Society.

Furthermore, it has been reported that for vacuum-deposited n-type organic semiconductors, the bias stability of OFETs is strongly dependent on the crystalline microstructure. Jung et al. reported n-channel organic semiconductors with high electron mobility and high bias stability; *N,N′*-bis(3-(perfluorooctyl) propyl)-1,4,5,8-naphthalene tetracarboxylic acid diimide (8–3-NTCDI) was molecularly designed and compared to other (perfluorooctyl)alkyl or alkyl side chains, as shown in **Figure 7**a.[56] In this study, they found that the enthalpy of the mesophase formation of N,N′-bis(3-(perfluorooctyl)alkyl)-1,4,5,8-naphthalene tetracarboxylic acid diimide depends strongly on the number of CH_2 subunits in the side chains: it is highest for the propyl unit (8–3-NTCDI), which leads to stronger intermolecular interactions. Thus, it was found that the 8–3-NTCDI-based thin film has the smallest interlayer spacing. This leads to the dependence of crystal orientation and molecular packing on the types of synthesized molecules. In particular, the 8–3-NTCDI thin film contains more laterally continuous growth than the N,N′-bis(3-(perfluorooctyl)butyl)-1,4,5,8-naphthalene tetracarboxylic acid diimide (8–4-NTCDI) thin film, as shown in Figures 7c and d. Stronger intermolecular interactions are expected to induce greater continuity, which results in reduced barriers to electron transport at grain boundaries and increased electron mobility. Figure 7b shows that the appropriate molecular design; fine control of the microstructure of these organic semiconductors strongly affects their threshold voltage shifts under ON and OFF gate bias stress, and can be used to produce high bias stability OFETs. Similarly, Wo et al. examined the effects of grain boundaries in in 6,13-bis(tri-isopropylsilylethynyl) pentacene (TIPS-PEN) semiconductors on bias stability, and found that shallow traps within disordered grain boundaries lead to negative effects on the stable operation of OFETs, even if this phenomenon is reversible.[68]

In summary, in this section we have examined recent reports of the impact of varying the crystalline microstructures of organic semiconductors on their bias stability in OFETs. These reports provide important insights into the control of crystalline microstructures for achieving stable OFET operation. High crystallinity, preferential orientation, large grain size, and high crystalline perfection are required of all types of organic semiconductors to ensure high electrical stability under bias stress because these properties minimize the number of charge traps in disordered regions. However, other factors such as the dielectrics and the characteristics of the interface between the channel and the dielectric components or between the channel and the S/D electrodes need to be considered at the same time. These considerations are discussed in Sections 3.2 and 3.3.

3.1.2. Effect of Molecular Design on Bias Stability in OFETs

Electrical stability under external bias stress can be simultaneously affected by extrinsic factors, such as oxidation, the presence of moisture, or chemical impurities, and also by intrinsic factors, such as microstructural disorder in the organic semiconductor or specific structural defects that enable charge trapping.[10] In particular, extrinsic factors are more sensitive to the electronic energy level (the HOMO level for p-type organic semiconductors and the LUMO level for n-type organic semiconductors) of the organic semiconductor than to its crystalline microstructure. As mentioned above, in order to accomplish electrical stability under bias stress as well as environmental stability, the molecular parameters of the organic semiconductor such as the electronic energy level and the density of states (DOS) should be simultaneously controlled. In this section, we review the effects of molecular design on bias stability for both vacuum-deposited and solution-processed organic semiconducting materials.

Interestingly, despite the disordered (i.e. amorphous) nature of the polytriarylamine (PTAA) organic semiconductor shown in **Figures 8**a and b, Mathijssen et al. reported the fabrication of OFETs with PTAA that are relatively stable in terms of the relaxation or characteristic time (τ) (Figure 8c), which implies that the characteristics of the crystalline phase are not the only factors in high bias stability. In other words, other factors are dominant in the bias stability of this semiconductor in OFETs.[11] Sharma et al. demonstrated that the bias stabilities of OFETs with a range of different organic semiconductors including PTAA, poly-dioctylfluorene-co-bithiophene (F8T2), polythienylenevinylene (PTV), pentacene, 3-butyl α-quinquethiophene (3-BuT5), and P3HT depend strongly on their HOMO energy levels.[12,69] The variation in the HOMO energy level originates

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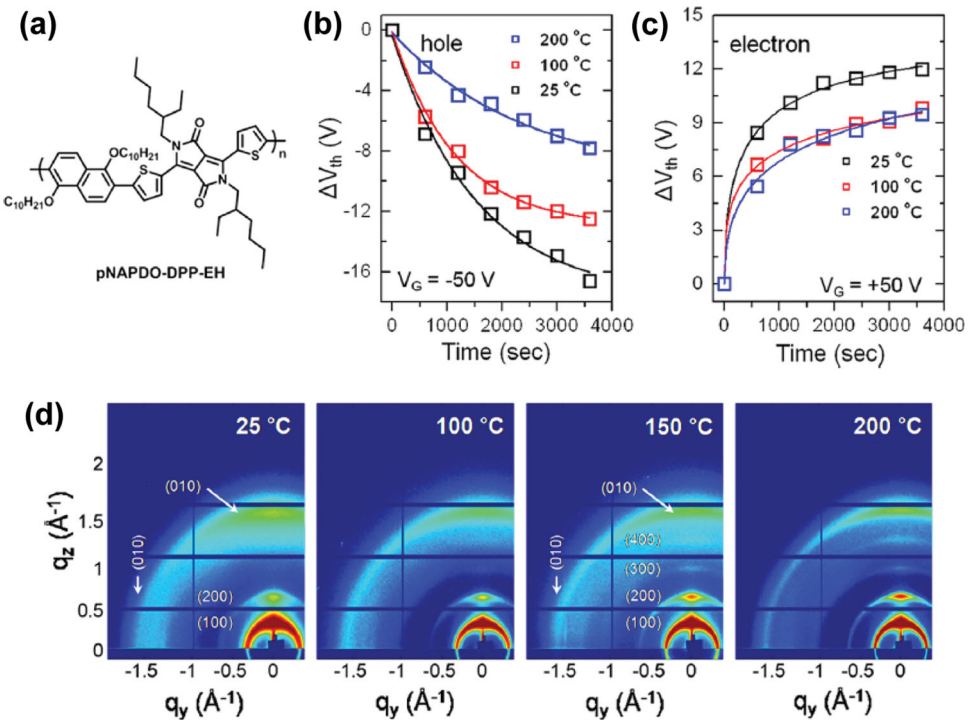

Figure 4. Effects of crystalline microstructure on the bias stability of a low band-gap pNAPDO-DPP-EH semiconductor. (a) Schematic diagram of the molecular structure of the pNAPDO-DPP-EH semiconductor. (b and c) Threshold voltage shifts of pNAPDO-DPP-EH-based OFETs as functions of bias-stress time for various annealing temperatures. (d) 2D GIXD patterns of pNAPDO-DPP-EH thin films for various annealing conditions. Reproduced with permission from ref [65]. Copyright 2013 American Chemical Society.

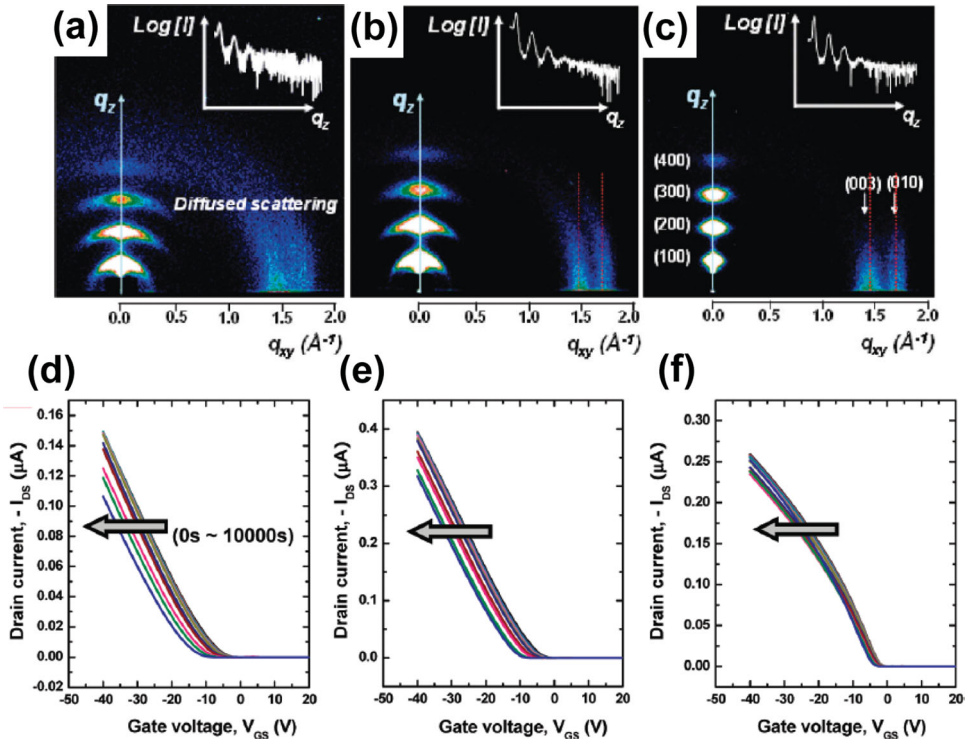

Figure 5. Effects of crystalline microstructure on bias stability in liquid-crystalline PQTBTz-C12 semiconductors. 2D GIXD patterns of the PQTBTz-C12 thin films spin-coated onto ODTS-treated SiO_2 substrates in terms of annealing conditions: (a) as-spun, (b) 100 °C, (c) 180 °C. Linear transfer curves of PQTBTz-C12-based OFETs as a function of stress time for various annealing temperatures: (d) as-spun (solid state), (e) annealed at 100 °C (solid state), and (f) annealed at 180 °C (mesophase). The gate bias (V_G) during stress was fixed at –20 V (on-state), and the temperature under operation was room temperature (drain bias (V_D) ≈ 0 V). Reproduced with permission from ref [58]. Copyright 2009 American Chemical Society.

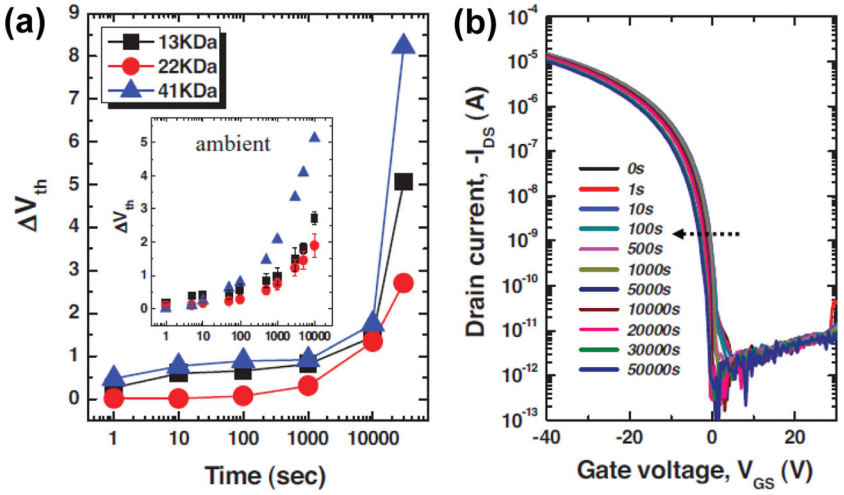

Figure 6. (a) Threshold voltage shift (ΔV_{th}) of PQTBTz-C12 FETs as a function of molecular weight (MW) under inert conditions (H_2O < 1 ppm and O_2 < 1 ppm): gate bias V_G: –20 V and drain bias V_D: –1 V). The inset shows ΔV_{th} measured under ambient conditions (RH ~40% at 25 °C) over a period of 10^4 s. (b) Transfer curves for a FET prepared with 22 kDa PQTBTz-C12 during prolonged bias stress (5×10^4 s) under ambient conditions. Reproduced with permission from ref [67]. Copyright 2011 Wiley.

from the variation in the molecular design of the chemical structures of the backbone or side-chains of these organic semiconductors. In particular, it was found that the relaxation time decreases with increases in the HOMO energy level. This result indicates that there is a strong correlation between the HOMO energy level and the bias stability, as shown in Figure 8d. Furthermore, Sharma et al. examined the influence of the HOMO energy levels of organic semiconductors on the dynamics of bias-stress effects in OFETs.[45] They found that with increases in the HOMO energy levels of organic semiconductors, proton production is increasingly favored, which results in exponential decreases in the characteristic time of the bias-stress effect. Since protons are produced in the oxidation of the organic semiconductor by atmospheric water, there should be a relationship between the rate at which the bias-stress effect develops and the HOMO energy level.

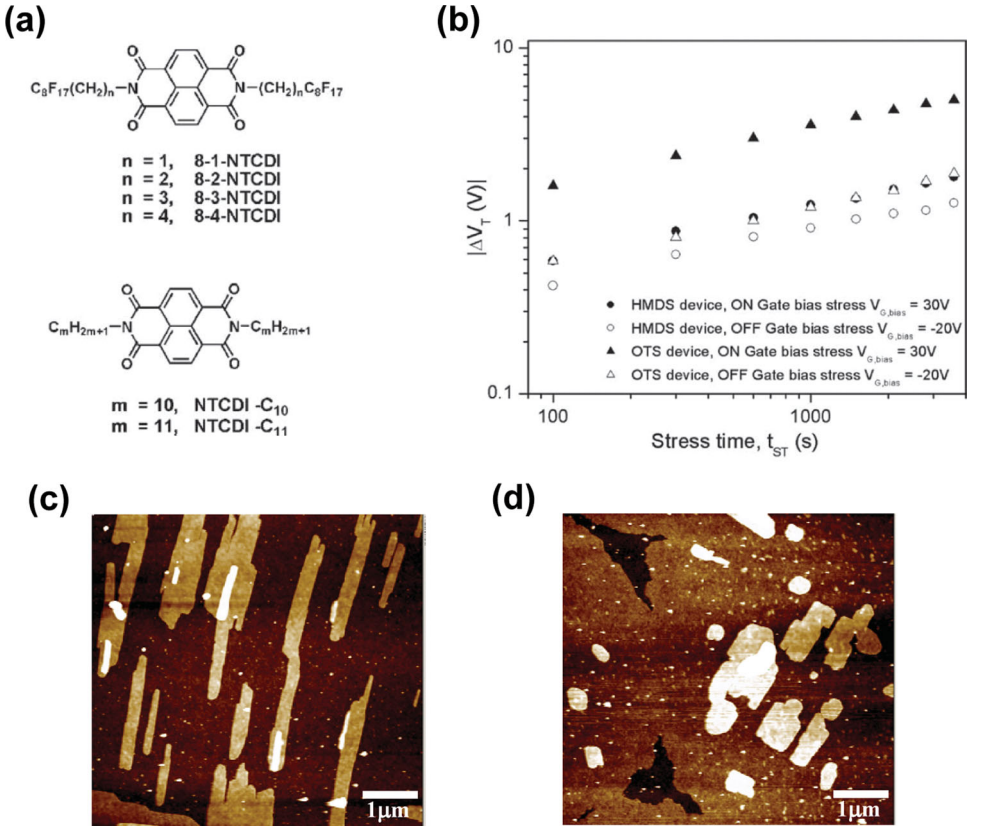

Figure 7. (a) Structures of N,N′-bis(3-(perfluorooctyl)alkyl)-1,4,5,8-naphthalene tetracarboxylic acid diimide and N,N′-dialkyl-1,4,5,8-naphthalene tetracarboxylic diimide. (b) Threshold voltage shift, ΔV_{th} as a function of stress time on a logarithmic scale (HMDS: hexamethyldisilazane, OTS: octadecyltrichlorosilane). AFM images of (c) 8–3-NTCDI and (d) 8–4-NTCDI films on OTS-treated substrates. The films were deposited at 120 °C. Reproduced with permission from ref [56]. Copyright 2010 Wiley.

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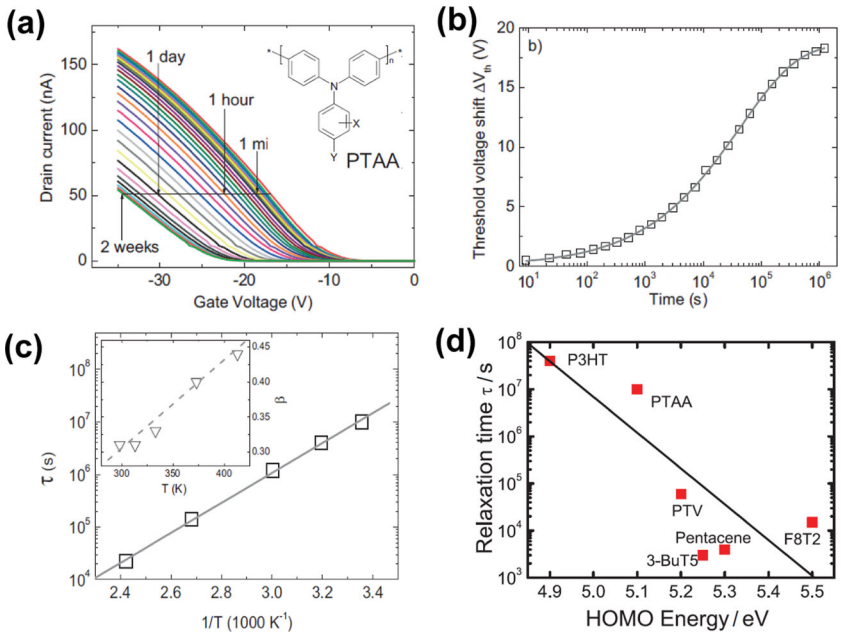

Figure 8. (a) Linear transfer curves of PTAA transistors as a function of stress time. The gate bias during stress was –20 V and the temperature 140 °C. (b) Threshold voltage shift, ΔV_{th}, as a function of time on a logarithmic scale. The fully drawn curve is a fit with a stretched-exponential time dependence. (c) Relaxation times, τ (s), as a function of reciprocal temperature. The inset shows the corresponding dispersion parameters, β, as a function of temperature. From the linear dependence, a characteristic temperature of the trap states of 9×10^2 K is obtained. Reproduced with permission from ref [11]. Copyright 2007 Wiley. (d) Relaxation times, τ (s) as a function of the energy of the highest occupied molecular orbital (HOMO) for four different polymeric semiconductors. Reproduced with permission from ref [45]. Copyright 2010 American Physical Society.

The fact that the time scale of the bias-stress effect decreases with increases in the HOMO energy level is further supported by the proton migration mechanism. In other words, in order to reduce bias instability, an organic semiconductor with a low HOMO energy level, preferably well below 5 eV, should be used, as shown in Figure 8d. However, with such a low HOMO energy level the semiconductor becomes unstable towards oxidation with respect to environmental stability, which indicates that a passivation layer is required to provide OFETs with both high bias and environmental stability.

In addition, Park et al. systematically synthesized indenofluorenediones (IF-dione) with various numbers of fluorine substituents, ranging from monofluoro (MonoF) to trifluoro (TriF), as shown in **Figure 9**a, for use in high mobility and high stability OFETs.[33] In this study, the electron-withdrawing properties of F atoms mean that their introduction onto the IF-dione backbone increases the electron affinity and lowers the LUMO level; the LUMO levels are –3.38 eV for MonoF-IF-dione and –3.53 eV for TriF-IF-dione. It was found that the threshold voltage shift of the TriF-IF-dione FETs is much smaller than that of the MonoF-IF-dione FETs, as shown in Figure 9b, which implies that the molecular design of these organic semiconductors strongly affects their bias-stress stability in OFETs. The parameters associated with the activation energy, i.e., E_A and k_BT, are summarized in Table 1: E_A is 0.477 eV for MonoF-IF-dione FETs and 0.629 eV for TriF-IF-dione FETs. The small values of the threshold voltage shift for the TriF-IF-dione FETs were attributed to higher activation energies for trap creation, which are due to the high electron affinity that reduces the possibility for electrons to be trapped because they are located on a lower LUMO level.

The effects on the bias stability of OFETs of the DOS should also be taken into account. Lee et al. demonstrated that the DOS near the band edge is enhanced by closer interchain packing in thiophene-based crystalline polymer semiconductors (i.e., P3HT, PQT-12, and PQTBTz-C12), which results in both higher field-effect mobility and higher bias stability.[41] They investigated this phenomenon by using *in situ* photo-excited charge collection spectroscopy (PECCS), which detects charge-induced absorption peaks from the delocalized polaron states. **Figure 10**a shows the DOS profiles of P3HT, PQT-12, and PQTBTz-C12; the absorption peaks of all the DOS profiles nearly overlap, which means that their intrinsic electronic properties are very similar even though the intensities of the spectra are different. However, there are large differences between the DOS values near the band edge of the polymer semiconductors: 0.65×10^{12} cm^{-2} eV^{-1}, 1.66×10^{12} cm^{-2} eV^{-1}, and 5.36×10^{12} cm^{-2} eV^{-1} for P3HT, PQT-12, and PQTBTz-C12, respectively, as shown in Figure 10a. These results demonstrate that the high crystallinity of the PQTBTz-C12 thin film results in high bias stability as well as high field-effect mobility (Figure 10b).

In summary, fine tuning the molecular design is essential to high bias stability in OFETs. In particular, control of the chemical structure of the backbone or side-chain can alter the HOMO or LUMO levels of p-type or n-type organic semiconductors, and thus change the bias stability. In addition, higher DOS values near the band edge lead to better bias stability, which is due to the resulting higher packing density or higher crystallinity of the organic semiconductor film.

3.2. Dielectric

Dielectrics and semiconductor-dielectric interfaces can also provide sites for charge trapping. Mathijssen et al. examined the surface potential profiles of FETs before/after the exfoliation of the organic semiconductor, PTAA (**Figure 11**).[70] They observed a typical negative V_{th} shift after an ON-bias stress of $V_G = -60$ V for 2 h (Figure 11a). After removing PTAA from the transistor, no FET characteristics were observed. On the other hand, the surface potential profile obtained with scanning Kelvin probe microscopy (SKPM) shows that a negative surface potential was present before bias stress (Figure 11b). This result is explained by electron trapping at the gate dielectric and is typical of OFETs with inorganic gate dielectrics.[11] The potential profile gradually shifts to positive values as the bias-stress time increases. This positive surface potential is

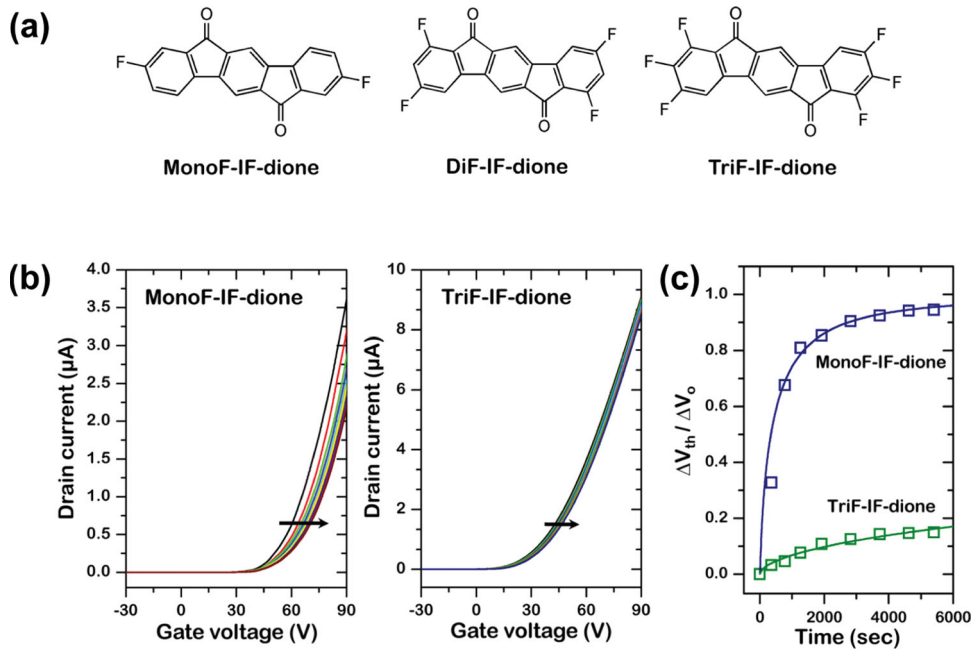

Figure 9. (a) Schematic diagram of structures of MonoF-IF-dione, DiF-IF-dione, and TriF-IF-dione. (b) Evolution of the linear transfer curves of MonoF-IF-dione FETs and TriF-IF-dione FETs based on Au source/drain contacts, as a function of bias stress time (0 ~ 90 min). The gate bias during stress was 50 V (On-state). (c) Plot of $\Delta V_{th}/\Delta V_0$ *vs.* bias stress time for the MonoF-IF-dione FETs and TriF-IF-dione FETs. The solid curves were fit to a stretched exponential equation. Reproduced with permission from ref [33]. Copyright 2011 American Chemical Society.

attributed to hole trapping at the gate dielectric (Figure 11c). PTAA was removed from the FETs and thus the semiconductor is not the location of charge trapping. Accordingly, hole trapping in the gate dielectric is one of the main reasons for the threshold voltage shift evident in Figure 11a.

Typically, inorganic dielectrics (i.e., SiO_2, Al_2O_3) or surface-modified inorganic dielectrics are used for examining the bias stability of OFETs (Table 1). These dielectrics are vulnerable to charge trapping because they contain ionic impurities.[71–73] In this regard, organic dielectrics are an alternative. The dielectric strengths and solvent resistances of common insulating polymers (i.e., PS, PMMA) are typically low, so cross-linked dielectrics are recommended. Hwang et al. examined the bias stability of pentacene FETs with a cross-linked polyvinylphenol (PVP) gate dielectric.[74] They compared the drain currents of two types of PVP with SiO_2 as a function of bias-stress time (**Figure 12**a). There is an increase in I_D for the partially cured PVP (15 min curing), while I_D is unchanged for the fully cured PVP (1 h curing) under ON-bias stress (V_G = V_D = −15 V). This result is in contrast with the result for SiO_2, for which I_D decreases as a function of stress time. Partially cured PVP contains many hydroxyl groups, which induce remnant dipoles due to their slow polarization characteristics.[75] In accordance with this report, Jung et al. examined the effects of water on the polarization characteristics of OFETs with a PVP dielectric.[76] They attributed the increases in $-I_D$ to the accumulation of extra charge carriers induced by the surface polarization of water. This result implies that the bias-stress effect in the partially cured PVP dielectric results from the uptake of water by hydroxyl groups.

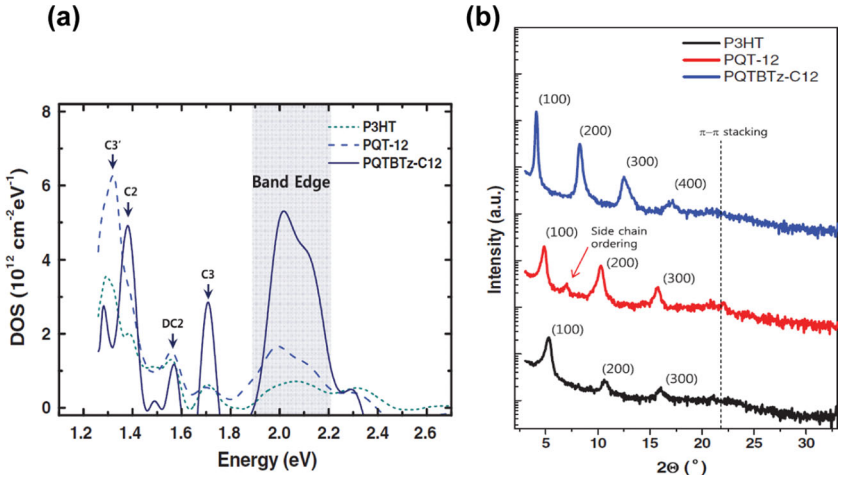

Figure 10. (a) The density of states (DOS) profiles and (b) XRD spectra of P3HT, PQT-12, and PQTBTz-C12. Reproduced with permission from ref [41]. Copyright 2012 American Physical Society.

Multilayer films are often recommended as providing gate-dielectric layers with high stability. Ng et al. investigated the stability of PQT-12 FETs with dual gate-dielectric layers comprising poly(methylsilsesquioxane) (pMSSQ) and either the epoxy resin SU-8 or PVP (Figure 12b).[77] pMSSQ was spin-coated on top of the other dielectric to render the

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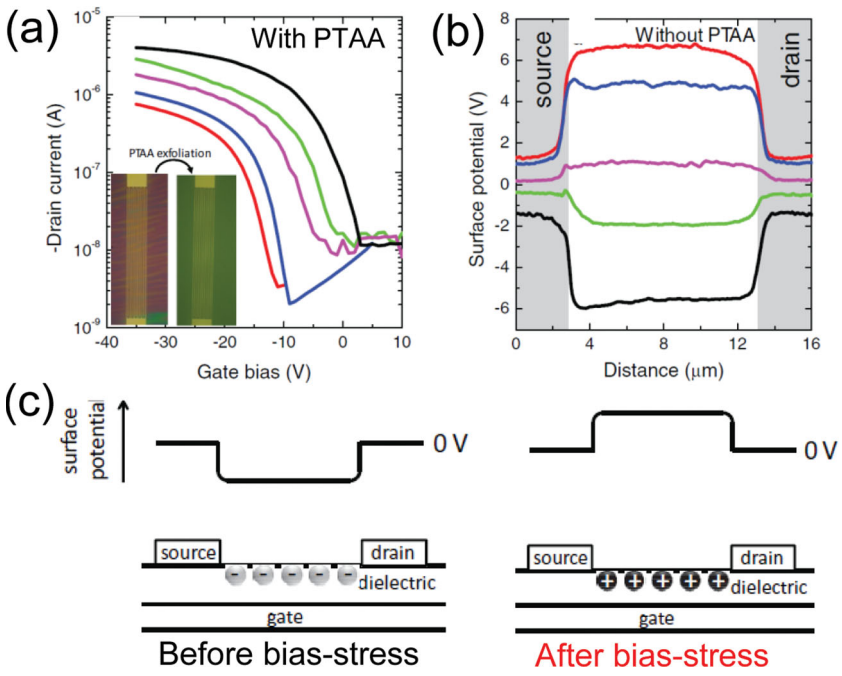

Figure 11. (a) Bias-stress driven shifts of the transfer curves before exfoliation of polytriarylamine (PTAA). Inset shows optical microscopy image of the FETs before (left) and after (right) PTAA exfoliation. (b) Corresponding surface potential profiles after PTAA exfoliation. The colors used in profiles correspond to curves in (a). (c) Schematics of the trapped charges in PTAA-removed FETs before (left) and after bias stress (right). Reproduced with permission from ref [70]. Copyright 2010 Wiley.

surface of the dielectric hydrophobic while providing the same dielectric-semiconductor interface. The current changes in the ON-bias stability results for 363 K and vacuum vary depending on the type of the underlying gate-dielectric layer. $-I_D$ increases for the pMSSQ/PVP dielectric, whereas it decreases for the pMSSQ/SU-8 and pMSSQ/PVP/SiO_2 dielectrics. Considering the measurement conditions (363 K, vacuum), the role of water can be ignored. Thus, the mechanism of slow polarization does not apply to the pMSSQ/PVP dielectric. Instead, charges injected from the gate into the dielectric raise the capacitance of the dielectric, which means that $-I_D$ increases during prolonged gate bias (Figure 12b upper right). For pMSSQ/SU-8 and pMSSQ/PVP/SiO_2 dielectrics, charge injection is prohibited and typical hole trapping can explain the decrease in $-I_D$ (Figure 12b lower right). According to these results, the stability of OFETs with a PVP/SiO_2 dielectric is dependent on the thickness of the underlying SiO_2 layer.[78] As the thickness of the SiO_2 layer increases, the hysteresis during the dual gate sweep decreases because charge injection from the gate is increasingly blocked by the SiO_2 layer.

High capacitance dielectrics have been widely investigated with the aim of reducing the operating voltages of OFETs.[4,79,80] Self-assembled monolayers (SAMs) constructed on oxide surfaces can be used to fabricate OFETs driven with low voltages.[79] Colleaux et al. examined the bias stabilities of OFETs with SAM nanodielectrics.[81] They used phosphonic acid SAMs with various end groups to fabricate FETs based on n-type/p-type organic semiconductors and compared their bias stabilities. Under ON-bias stress, ΔV_{th} shifts to positive values for n-type FETs whereas ΔV_{th} shifts to negative values for p-type FETs. These results can be satisfactorily fitted with the charge-trapping-induced stretched-exponential equation. Interestingly, the end groups of the SAMs also influence the bias stabilities of the FETs, which demonstrates that both the dielectric-semiconductor interface and the semiconductor play important roles in charge-trapping phenomena. Polyelectrolyte-gated OFETs have also been tested with the aim of enabling low-voltage operation.[4,82] Sinno et al. investigated the effects of bias stress on OFETs with poly(styrene sulfonic acid) (PSSH) dielectrics.[51] They found that the negative ΔV_{th} response of the OFETs to negative V_G stress was six orders of magnitude faster than that of a typical dielectric. This fast charge trapping was explained in terms of the migration of protons into the PSSH polyelectrolyte.

Even when the same dielectric is used, the chemical and physical structures of the dielectric can affect bias stability. In particular, the molecular weight (MW) and polydispersity index (PDI) of the polymeric dielectric can vary. Choi et al. investigated the effects of varying the MW of a PS gate dielectric on the bias stability of the associated OFETs (**Figure 13**).[29] PS samples with MWs ranging from 8 to 500 kDa with PDI ≤ 1.05 were used as the gate dielectrics and the other layers of the pentacene FETs were identical. The field-effect mobilities of the FETs and the morphologies of pentacene do not vary significantly with MW. Under ON-bias stress (V_G = −60 V, V_D = −5 V) in ambient air, however, the I_D decay is highly dependent on the PS MW: the FET with PS with the highest MW exhibits the least I_D decay (Figure 13a). In contrast, the I_D decay is independent of MW under vacuum measurement conditions. Thus, the effects of varying MW on bias stability can be explained in terms of the bulk properties of PS related to water. The free volume at the PS chain-ends is sufficiently large to allow the adsorption of water molecules, which means that charge carriers can be trapped in water-filled trap sites (Figure 13b). This effect is magnified for PS with low MW. The plot of the trapping frequency ω vs PS chain-end density ρ shows that the density of trap sites increase as ρ increases (or MW decreases) (Figure 13c). In a further experiment, the end groups of PS chains were also found to influence bias stability. The FET with H end-terminated PS was found to be much more stable than the FET with COOH end-terminated PS under humid N_2 conditions. This result also confirms that charge carriers can be trapped at polymer chain ends with adsorbed water molecules. Trap sites can readily be formed within the dielectric layer, so the chemical and physical structures of the dielectric as well as the type of the dielectric must be taken into account in the fabrication of high stability OFETs.

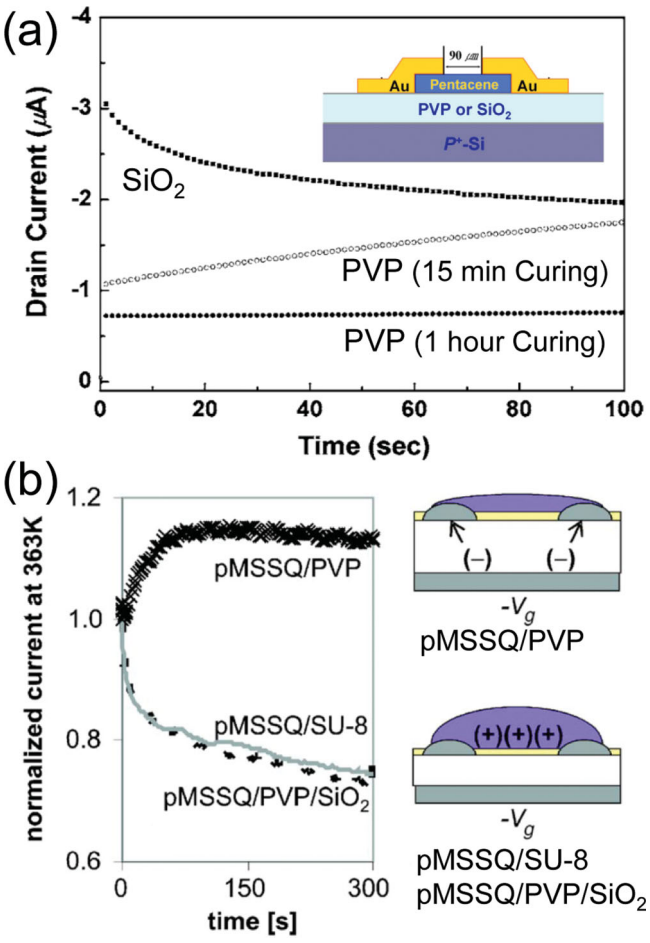

Figure 12. (a) Timed-dependent I_D characteristics under a gate bias stress of $V_G = V_D = -15$ V. Pentacene was used as a semiconductor and different dielectrics were used for comparing the gate-bias effect. Reproduced with permission from ref [74]. Copyright 2006 American Institute of Physics. (b) Normalized I_D at 363 K in vacuum for PQT-12 FETs with different dielectrics. $V_D = -5$ V, $V_G = -20$ V (pMSSQ/PVP and pMSSQ/SU-8), $V_D = -5$ V, $V_G = -30$ V (PMSSQ/PVP/SiO_2). The cartoons illustrate the bias-stress mechanism for different dielectrics. Reproduced with permission from ref [77]. Copyright 2008 American Institute of Physics.

3.3. Semiconductor/Dielectric Interface

It has been reported that water molecules on a SiO_2 dielectric can trigger charge trapping, thereby inducing bias-stress instability. In this regard, the surface treatment of SiO_2 with a silane coupling agent can be an effective method of reducing bias-stress instability. Goldmann et al. reported the enhancement of the bias stability of pentacene single crystal FETs after treating the SiO_2 surface with octadecyltrichlorosilane (OTS) (**Figure 14**a).[83] Under ON-bias stress ($V_G = -60$ V, 100 min), a step-like feature is evident in the variation of I_D for the FET with untreated SiO_2; this feature is absent for the FET with OTS-treated SiO_2. The formation of discrete trap states is minimized by the presence of the hydrophobic OTS layer. Similarly, the interface trap density in rubrene single crystal FETs can be reduced by the use of OTS SAMs.[84] The trap density of the rubrene/SiO_2 interface is twice that of the rubrene/OTS/SiO_2 interface and is approximately three orders of magnitude higher than the bulk trap density of organic single crystals. These results show that the semiconductor-dielectric interface must be carefully adjusted to fabricate high stability FETs based on organic single crystals.

Interface quality is also important for FETs based on polycrystalline semiconductor films. Miyadera et al. investigated the effects of β-phenethyltrichlorosilane (β-PhTS) treatment on the bias stabilities of FETs based on evaporated pentacene films (Figure 14b).[30] Two different evaporation rates (0.01 and 0.1 nm/s) were used in the deposition of pentacene to examine the effects of grain size. The evaporation rate of pentacene was found to have little influence on the current decay upon prolonged gate bias; in other words, the pentacene film morphology has little influence on trapping phenomena. After β-PhTS treatment of the SiO_2 surface, the current decay upon bias stress was significantly reduced (Figure 14b). In addition, the charge-trapping activation energy E_A was calculated to be ~ 0.4 eV, which is much higher than that for untreated SiO_2, ~ 0.08 eV. This significant increase in barrier height is attributed to the β-PhTS buffer layer on the SiO_2 surface.

SAMs have also been reported to have disadvantageous effects on bias stability. Ng et al. examined the effects of OTS treatment on the bias stability of FETs based on F8T2 and PQT-12 films.[85] For these solution-processed films, the E_A of OTS-treated SiO_2 was found to be much lower than that of untreated SiO_2. This result indicates that the kinetics of trap formation and release are faster for OTS-treated SiO_2 than for untreated SiO_2. Suemori et al. studied SAMs with various alkyl chain lengths to examine the effects on bias stability of chain length.[47] As the alkyl chain length increases, ΔV_{th} increases upon ON-bias stress ($V_G = -20$ V, 1 h). This result is in accordance with the results of Ng et al., who reported the lowering of the E_A of OTS-treated SiO_2. Why does surface treatment with SAMs result in opposing effects? We speculate that the phase state, such as the order or disorder, and the density of SAMs can both affect bias stability.[86,87] In this regard, the SAM preparation procedures of the two sets of experiments might have been different, and thus have resulted in SAMs with different phase states and densities. Further, the impurities in the inorganic dielectrics, such as SiO_2, on which the SAMs were constructed were different in each experiment, thereby dispersing bias stability of untreated SiO_2. Thus, it is not easy to determine whether individual SAMs have advantageous (or disadvantageous) effects on bias stability. Further studies of well-organized SAMs on well-established inorganic dielectrics are necessary to properly investigate the effects of SAMs on bias stability.

Recently, Gholamrezaie et al. examined the effects of the end groups of SAMs on charge-trapping behaviors in the channel region.[88] Surface potential measurements with SKPM have unambiguously demonstrated that charge trapping is permanently induced by the end groups of SAMs. Negative surface potential is induced in F-SAMs with electron-withdrawing character whereas positive surface potential is induced in NH_2-SAMs with electron-donating character.[89–92] In nonpolar CH_3-SAMs, on the other hand, the surface potential across the active channel is negligible. This result underlines the importance of the careful use of SAMs in enhancing the bias stability of OFETs because polar SAMs can be charge-trapping sites.

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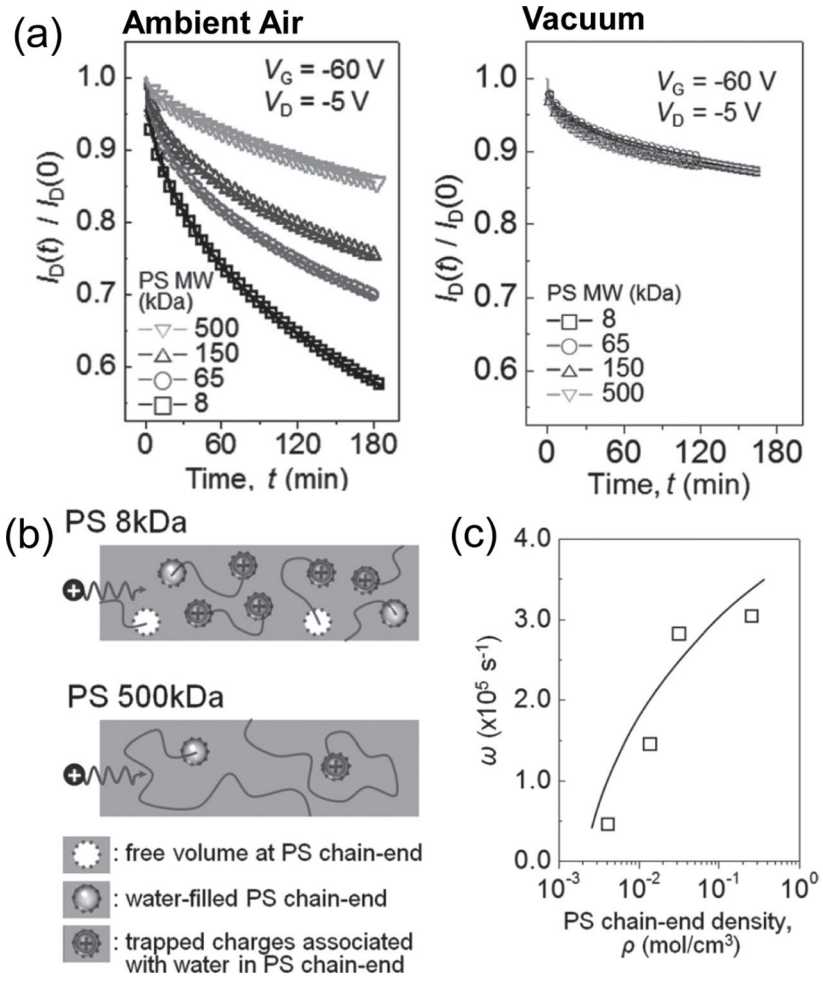

Figure 13. (a) Time dependent I_D characteristics of pentacene FETs under a gate bias stress (V_G = −60 V, V_D = −5 V) in ambient air (Left) and vacuum (Right). PS with different molecular weight (MW) was used as a dielectric. (b) Schematic diagrams showing a possible mechanism for the MW-dependent bias stability. (c) Plot of ω vs PS chain-end density ρ. Reproduced with permission from ref [29]. Copyright 2012 Wiley.

Polymer brushes can also serve as efficient surface modifiers for SiO_2.[54,93–95] Park et al. enhanced the bias stability of triethylsilylethynyl anthradithiophene (TES-ADT) FETs by using "grafting to" polymer brush.[54] They compared the effects of adding a polymer brush to those obtained with OTS and found that the crystal perfection of the solvent-annealed TES-ADT is higher with a grafted polymer brush than with OTS. The mobile chains in the polymer brush influence the crystallization of TES-ADT under solvent annealing, thereby enhancing crystal perfection. The ON-bias stability of the FET with the polymer brush was greatly enhanced by the combined effects of the enhanced crystal orientation and the quality of the semiconductor-dielectric interface.

The roughness of the interface between the semiconductor and the dielectric can also affect bias stability. Suemori et al. investigated the influence of the surface roughness of the dielectric on the bias stability of pentacene FETs.[96] A small increase in the RMS roughness from 0.16 nm to 0.22 nm results in an abrupt increase in ΔV_{th} from −3.5 V to −10.3 V. This huge change is attributed to lattice distortion in the pentacene film evaporated onto the rough SiO_2 surface. Pentacene cannot form a uniform monolayer on a rough dielectric. As a result, the grain size of pentacene decreases and there is lattice distortion in the pentacene layer. Impurities such as oxygen and water can then invade the distorted pentacene layer, which offers an increased number of charge-trapping sites. The roughness effect addressed in this study was related to the growth characteristics of pentacene evaporated on a rough dielectric. In this regard, intrinsic roughness effects at the semiconductor-dielectric interface also need to be addressed to enhance our understanding of interface effects on bias stability.

Organic semiconductor-insulating polymer blends have been studied with the aim of improving the device performances of OFETs.[97–105] Environmentally stable, low-voltage-driven, and high-performance OFETs have been demonstrated when the appropriate phase separation of the blends is performed. This approach using polymer blends is also applicable to bias stability. Lee et al. enhanced the bias stability of some FETs by using active layers consisting of PQTBTz-C12:PMMA blends.[106] The FET with a PQTBTz-C12:PMMA blend film exhibits better OFF (positive) bias stability than the FET with PQTBTz-C12 (**Figure 15**a). The ON (negative) bias stability was nearly the same in both cases. It was proposed that the carboxyl groups in PMMA suppress hole accumulation in the channel region, thereby delaying turn-on voltage degradation and increasing OFF-bias stability (Figure 15b). The blend film discussed in this report consists of a PMMA top layer and a PQTBTz-C12 bottom layer and its structure is mainly due to the solubility differences in chlorobenzene (CB). The phase-separated structure can be varied by using different organic semiconductor-insulating polymer pairs. Lee et al. used difluorinated triethylsilylethynyl anthradithiophene (F-TESADT)/PMMA blends to investigate bias-stress effects (Figure 15c).[107] In this system, F-TESADT has a lower surface energy and so is segregated at the air-film interface. The phase-separated structure is dependent on the solvent used in the preparation of the blend solution. The blend film prepared in 1,2-dichlorobenzene (DCB) contains F-TESADT with a higher crystallinity and a smoother interface between F-TESADT and PMMA than the blend film prepared in CB. Accordingly, the ON-bias stability of the FET with the blend film prepared in DCB is superior to that of the FET with the blend film prepared in CB. These stabilities are much better than the stability of the FET based on the homo F-TESADT film. Although the phase-separated interface between F-TESADT and PMMA in the blend film prepared in DCB is rather rough with an RMS roughness of 2 nm, an excellent pathway for charge

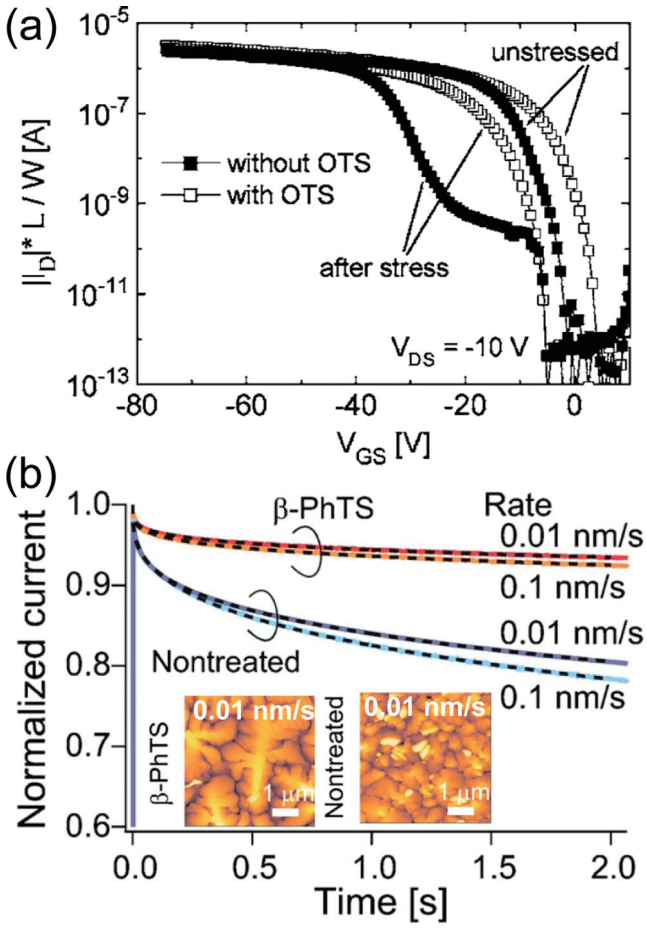

Figure 14. (a) The performances of pentacene single crystal FETs, one with an untreated SiO_2 dielectric surface and one with an OTS-treated dielectric surface, before and after bias stress (V_G = –60 V for 100 min). With permission from ref [83]. Copyright 2006 American Institute of Physics. (b) Time-dependent I_D characteristics of pentacene FETs with or without SiO_2 surface treatment (untreated vs β-PhTS-treated). V_G was varied from V_G = 0 V to V_G = –10 ~ –40 V, and this condition was maintained for 2 s at a constant V_D of –1 V. Two different rates (0.01 and 0.1 nm/s) of deposition of pentacene were used to fabricate the semiconducting layers. The insets show AFM images of the pentacene films obtained at a constant deposition rate of 0.01 nm/s. Reproduced with permission from ref [30]. Copyright 2008 American Institute of Physics.

transport is guaranteed at the phase-separated interface. This result indicates that roughness itself might not affect bias stability significantly and that the quality of contact between the semiconductor and the dielectric is much more important.

There are several charge-trapping sites in the layered structures of OFETs. In this review, the roles of the semiconductor, the dielectric and the semiconductor-dielectric interface in charge trapping have been discussed. In addition to these sites, source/drain contacts where the source/drain electrodes are in contact with the semiconductor can also be involved in charge trapping.[108] During charge injection, charge trapping can take place near the contact. In this regard, the device configuration (i.e., bottom-contact or top-contact) can also affect bias stability.[109]

Charge-trapping events generally take place at the interface between the semiconductor and the dielectric. Thus, it makes sense to separate the contributions to charge trapping of the semiconductor side of the interface and the dielectric side of the interface. Choi et al. decoupled these two contributions to bias-stress-induced charge trapping by fabricating two separated OFETs that shared a common semiconductor, P3HT, but were independently operated with SiO_2 or vacuum gap dielectrics (**Figure 16**, top image).[34] In the FET with a vacuum gap dielectric, charge trapping on the dielectric side of the interface was minimized and only the semiconductor side of the interface contributes to charge trapping. The contribution from the dielectric side of the interface to charge trapping can be extracted (curve C in Figure 16) from the bias-stability results for the devices shown in curves A and B by using a double stretched-exponential formula.

The vacuum serves as a trap-free gate dielectric, and an organic single crystal is a trap-free semiconductor. It has been reported that charge carriers are predominantly trapped at the grain boundaries of polycrystalline films. Thus, an organic single crystal without any defects can be used as a semiconducting layer in high-stability OFETs. The measurement conditions are very important in tests of organic single crystal FETs because water and oxygen molecules can diffuse into the crystal and destroy its chemical and physical structures, thereby creating trap sites inside the crystal. Kalb et al. used a rubrene single crystal and a fluoropolymer (Cytop) as the semiconductor and dielectric respectively to fabricate high-stability OFETs.[62] Remarkably, their transistor was found to exhibit negligible ΔV_{th} shifts under ON-bias and OFF-bias stresses and inert helium conditions (Figures 2a, b). This example demonstrates that a high degree of bias stability can be achieved by using both a defect-free single crystal and a robust gate dielectric. Cytop is a low-k gate dielectric that is highly water-repellent, and is thus ideal for high-stability OFETs.[62,63] It is not clear that this dielectric acts as a trap-free gate dielectric with other organic semiconductors, but it was shown that the performance of this polymeric gate dielectric is comparable to that of a vacuum gate dielectric in this system.

4. Conclusions and Perspectives

Recent studies have shown that gate- or drain-bias-induced V_{th} shifts and the current decays of OFETs can be fitted by using the stretched-exponential equation in analogy with a-Si:H. However, the origins of bias stability in OFETs are totally different from those of a-Si:H mainly due to the differences between the charge-trapping phenomena. We have discussed three main sites of bias-stress-induced charge-trapping in OFETs: semiconductors, gate dielectrics, semiconductor-dielectric interfaces. The various features of the crystalline microstructures of organic semiconductors, such as crystallinity, molecular orientation, and grain size, can be controlled by varying the molecular design and/or the processing conditions in order to modify or eliminate structural defects that enable charge trapping and thus enhance bias stability. In the case of molecular design, the features of the electronic structure of a synthesized organic semiconductor, such as the HOMO or LUMO levels or DOS, can be varied by introducing functional groups into the chemical structure. However, a general relationship between the

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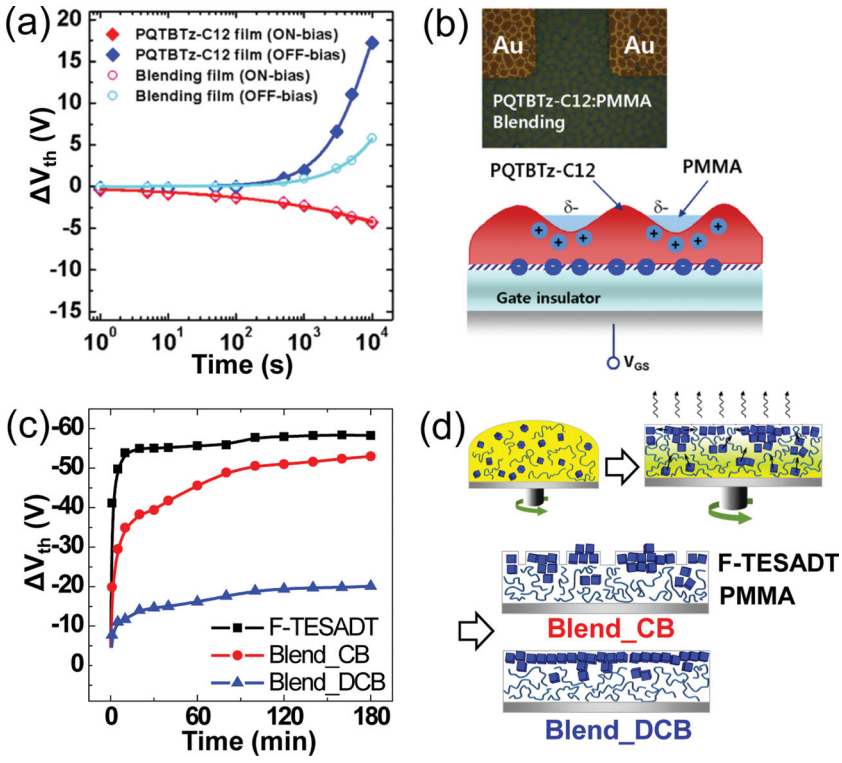

Figure 15. (a) The threshold voltage shift (ΔV_{th}) as a function of stress time for ON-bias ($V_G = -20$ V) and OFF-bias ($V_G = 20$ V) conditions at $V_D = -20$ V. (b) Optical microscopy image of PQTBTz-C12:PMMA blend film (top) and schematic cross-section showing negative dipoles of carboxyl groups in PMMA, which prevent hole accumulation at the PQTBTz-C12:PMMA blend active layer. Reproduced with permission from ref [106]. Copyright 2012 American Institute of Physics. (c) ΔV_{th} as a function of stress time at $V_G = -60$ V and $V_D = -5$ V. (d) Schematic representations of the variations in the F-TESADT-top/PMMA-bottom blend films spin-cast from chlorobenzene (CB) and 1,2-dichlorobenzene (DCB). Reproduced with permission from ref [107]. Copyright 2012 Wiley.

electronic structure and the bias stability has not yet been established because crystalline microstructure is also dependent on the chemical structure of the organic semiconductor. In this regard, the microstructural effects must be separated from the effects of electronic structure in order to synthesize stable organic semiconductors with low bias-stress effects and thus obtain OFETs with high bias stability. The importance of charge trapping at grain boundaries indicates that minimizing grain boundaries is a rational approach to reduce the bias instability of OFETs with polycrystalline films.[110,111] On the other hand, it is also necessary to investigate the bias stabilities of OFETs with amorphous-like organic semiconductors, because it has been demonstrated recently that some organic semiconductors with high electrical stability have low crystallinity.[8,15,112] As organic single crystals can serve as ideal trap-free semiconductors, chrage trapping at the gate-deielctric and interface between semiconductor and gate-dielectric can be determined by using organic single crystal FETs.[113]

Charge trapping at the gate dielectric has been demonstrated with surface potential measurements after the removal of the semiconductor; such charge trapping results in bias instability that depends on the type of gate dielectric. Typically, the charge-trapping phenomena of organic gate dielectrics are totally different from those of inorganic gate dielectrics. In particular, the bias-stress instability of polymer gate dielectrics has a strong dependence on the chemical and physical structure of the dielectric (i.e., molecular weight, chain end groups). Then, what are the recommended chemical and physical structures for electrically stable polymer gate dielectrics? For a cross-linked polymer, the number of unreacted chemical groups such as hydroxyl groups should be minimized because they can trigger charge trapping. Fluoropolymers such as Cytop can be utilized to fabricate electrically stable OFETs because fluorine groups have water-repellent characteristics. When selecting a suitable gate dielectric, however, device architecture and processing method should also be taken into account. For instance, in most cases the Cytop dielectric is fabricated with a top-gate structure in which the dielectric is placed onto the semiconductor. Note that the solution processing of an organic semiconductor onto a Cytop dielectric results in dewetting of the solution. Furthermore, the gate dielectric should be selected in combination with the organic semiconductor. Previous studies have shown that the charge carrier mobility can be optimized by selecting a specific semiconductor-dielectric pair. Such optimization is also likely to be applicable to bias stability. Further studies of this relationship are needed.

The density of interface charge trapping has been reported to be higher than the bulk trap density at gate dielectrics, so surface treatment and the control of the interface roughness of gate dielectrics can affect bias instability. Some studies have examined the effects of SAMs on bias stability, but further studies that employ well-organized SAMs are necessary to disentangle the effects of surface treatment.[30,34,70,88,114] In addition, the effects of the interface roughness of the gate dielectric need to be both theoretically and practically clarified. The interface roughness is inevitably high in OFET fabricated on plastic substrate, and thus electrical stabilities of the OFETs should be insensitive to the interface roughness for plastic electronics. Recent studies that have utilized organic semiconductor/insulating polymer blends to fabricate the semiconductor and gate dielectric simultaneously have shown that a rough interface does not decrease either the carrier mobility or the bias stability. Note that in one study it was found that charge carriers pass through the phase-separated rough interface (RMS roughness of ~2 nm) between the organic semiconductor and the insulating polymer.[107] These results show that it is possible that the effects of roughness on bias instability might not be significant for plastic electronics.

The passivation of OFETs is very important for their long-term environmental stability. Organic semiconductors are especially vulnerable to H_2O and/or O_2 under atmospheric

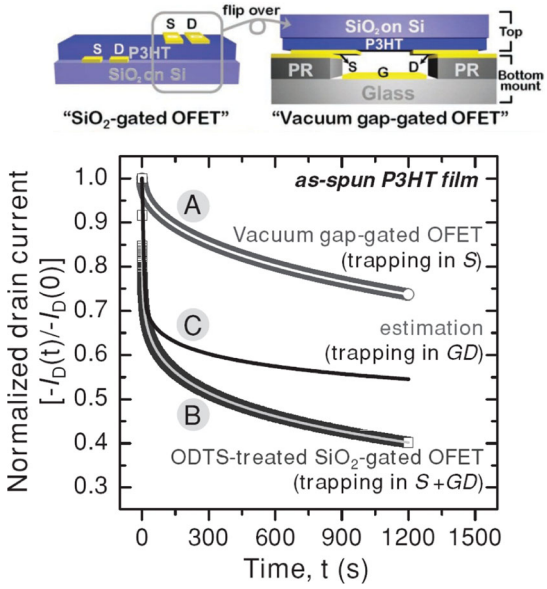

Figure 16. Normalized current decay for the vacuum gap FET (A) and the ODTS-treated SiO_2 FET (B). The current decay in A indicates charge trapping in the semiconductor layer-side (S) of the interface, whereas the current decay in B indicates charge trapping in both the semiconductor layer-side of the interface and the gate-dielectric layer-side (GD) of the interface. Curve C represents the current decay from the charge traps located in the GD of the interface, which is extracted from the double stretched-exponential formula. Schematic diagram of the bottom-contact P3HT FETs with SiO_2 and vacuum gap dielectrics is shown in upper panel. Reproduced with permission.[34] Copyright 2013 Wiley.

conditions. Bias stability is also affected by passivation as the origins of bias-induced charge trapping are closely related to the fates of these atmospheric molecules. The effects of passivation on bias stability need to be extensively examined in order to fabricate OFETs with high environmental and electrical stabilities. Although we have examined the distinct origins of bias instability, bias-stress-driven charge trapping is a complex phenomenon that depends on a subtle interplay between the layers of OFETs. In addition, bias stability is also dependent on the design of circuits. In one study, complementary inverters exhibited better bias stabilities than unipolar inverters.[115] In this regard, bias stability of organic transistors needs to be examined in connection with the design of circuit. We believe that detailed analysis of charge-trapping mechanisms can reveal the origins of bias-stress instability and that future endeavors to reduce bias instability will enable practical applications of OFETs in flexible flat panel displays.

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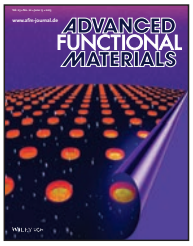

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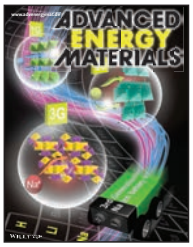

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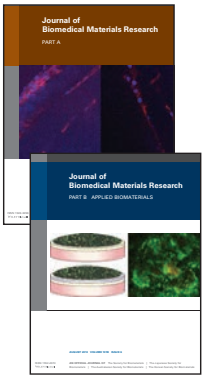

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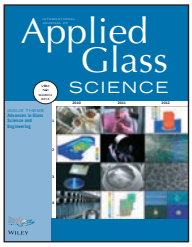

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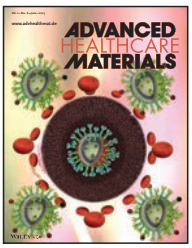

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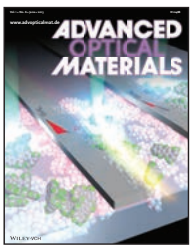

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