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Three-Dimensional, Inkjet-Printed Organic Transistors and Integrated Circuits with 100% Yield, High Uniformity, and Long-Term Stability

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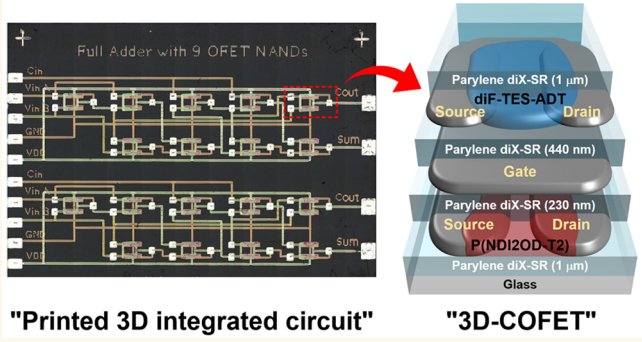
S *Supporting Information*

ABSTRACT: **In this paper, we demonstrate three-dimensional (3D) integrated circuits (ICs) based on a 3D complementary organic field-effect transistor (3D-COFET). The transistor-on-transistor structure was achieved by vertically stacking a p-type OFET over an n-type OFET with a shared gate joining the two transistors, effectively halving the footprint of printed transistors. All the functional layers including organic semiconductors, source/drain/gate electrodes, and interconnection paths were fully inkjet-printed except a parylene dielectric which was deposited by chemical vapor deposition. An array of printed 3D-COFETs and their inverter logic gates comprising over 100 transistors showed 100% yield, and the uniformity and long-term stability of the device were also investigated. A full-adder circuit, the most basic computing unit, has been successfully demonstrated using nine NAND gates based on the 3D structure. The present study fulfills the essential requirements for the fabrication of organic printed complex ICs (increased transistor density, 100% yield, high uniformity, and long-term stability), and the findings can be applied to realize more complex digital/analogue ICs and intelligent devices.**



KEYWORDS: *complementary organic field-effect transistor, inkjet printing, printed integrated circuit, 3D circuit, full adder*

The direct printing of organic field-effect transistors (OFETs) has received considerable attention for the realization of low-cost, large-area, and flexible circuits and systems.[1,2] Among various printing techniques, drop-on-demand inkjet printing is considered as a key enabling technology because of its unique features such as its digital, noncontact printing process and the ability to deposit a wide range of materials.[3,4] Since the first demonstration of an inkjet-printed OFET,[5] various passive and active electronic devices have been inkjet-printed, including resistors,[6,7] light-emitting diodes,[8,9] solar cells,[10,11] photodetectors,[12,13] transistors, and circuits.[14−17] However, despite the significant enhancements in the field-effect mobilities of organic semiconductors (OSCs) to greater than 10 $cm^2\ V^{-1}\ s^{-1}$ in recent years,[18,19] few attempts have been made to print complementary organic integrated circuits (ICs), such as binary arithmetic circuits. Without the realization of such demanding circuit applications by inkjet printing, this technique will not enter the advanced stages of industrial commercialization. To make this technique viable, high transistor density, 100% yield, uniform operation, and long-term stability must be achieved; however, no previous work has met all these requirements.

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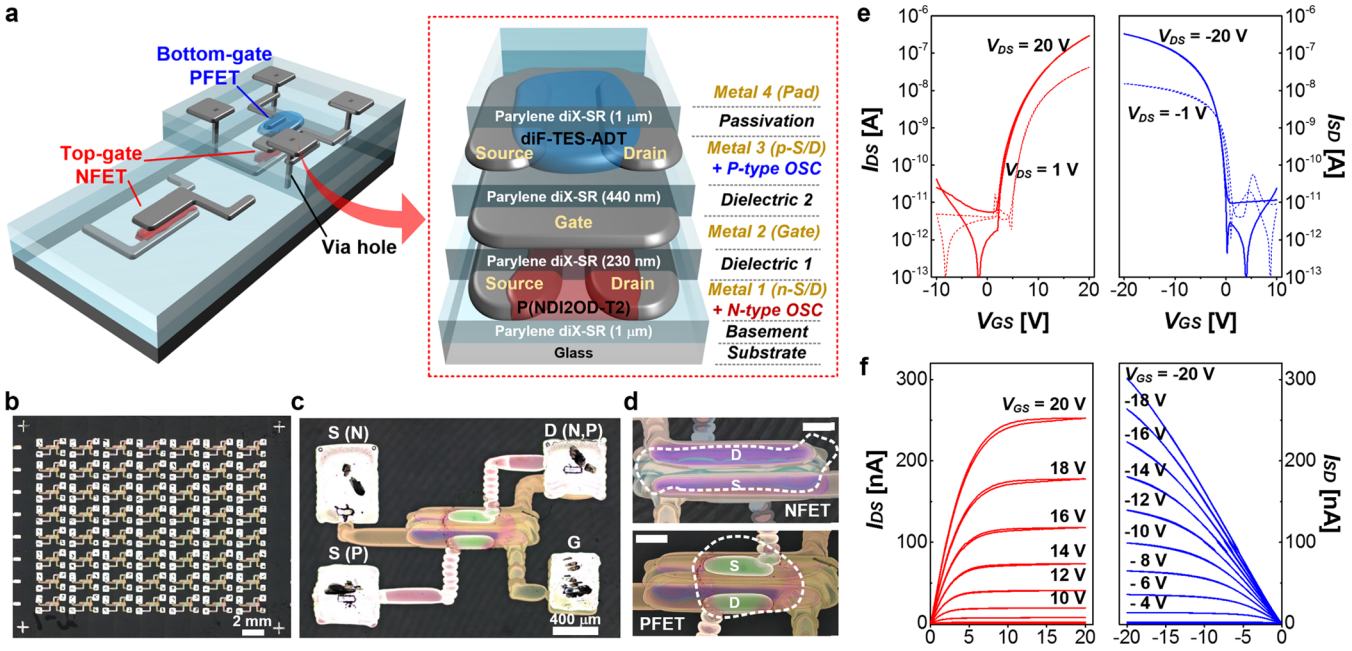

Figure 1. (a) Three-dimensional schematic cross section of the 3D-COFET with a bottom-gate PFET vertically stacked on a top-gate NFET. (b) Top view of 56 pairs of 3D-COFET inverters fabricated by inkjet printing on a substrate (S, source; D, drain; G, gate). (c) Microscope images of a 3D-COFET inverter and (d) printed active regions (white dotted areas) observed from the bottom (NFET) and the top (PFET) FETs by optical microscopy (scale bars = 200 μm). (e) Transfer characteristics ($|I_{DS}|$ *vs* V_{GS}) and (f) output characteristics ($|I_{DS}|$ *vs* V_{DS} with 2 V step V_{GS}) of the NFET (red, left graphs) and the PFET (blue, right graphs).

The low resolution (typically 20−50 μm) and large feature size (typically 50−200 μm) of inkjet printing have limited the implementation of organic ICs with reasonable transistor densities.[2,20] To overcome the above limitation, attempts to improve performance by downscaling have been employed by the silicon transistor industry for the last 40 years.[21,22] Alternatively, the three-dimensional (3D) integration of transistors offers a promising solution for cramming more components onto ICs by both reducing the effective device size and optimizing interconnect paths. Several attempts have been made to build 3D organic transistors, including a vertically stacked bottom-gate pentacene transistor with an electrical isolation layer,[23] a stacked bottom-gate pentacene transistor with varying threshold voltages,[24] and a complementary organic transistor with a shared gate electrode.[25] These studies mainly used high-vacuum or high-temperature fabrication processes that are inapplicable to the roll-to-roll manufacturing of low-cost and large-area electronics. Recently, solution-processed and inkjet-printed organic transistors with transistor-on-transistor structures have been demonstrated.[26,27] Although these two approaches were shown to be effective for enhancing transistor density, previous studies did not investigate the yield, uniformity, and long-term stability, and therefore, they cannot be extended to large-scale ICs beyond the level of a single logic gate.

In this study, we demonstrated organic digital ICs based on 3D complementary OFETs (3D-COFETs). A roll-to-roll-compatible, drop-on-demand inkjet-printing technique has been adopted for the precise patterning of silver source/drain (S/D) and gate metal electrodes and organic semiconductor materials. The 3D-integrated COFETs were achieved by stacking a p-type OFET (PFET) over an n-type OFET (NFET) with a shared gate joining the two transistors, which doubled the number of transistors printed per unit area. An array of printed 3D-COFETs and their inverter logic gates comprising over 100 transistors have shown a 100% yield, and the uniformity and long-term stability of the device were also investigated. A full-adder circuit, the most basic computing unit, has been successfully demonstrated using nine NAND gates based on the 3D structure. The present study fulfills all the unmet requirements mentioned above for the fabrication of organic printed complex ICs, and the findings can be applied to realize printed wearable computers.

RESULTS AND DISCUSSION

The organic ICs for the computing device studied in this work were based on COFETs with the vertical configuration of two p- and n-type transistors. The 3D-COFET was achieved by stacking a bottom-gate top-contact PFET on top of a top-gate bottom-contact NFET with a shared gate electrode between the two FETs. This 3D-configured COFET is particularly suitable for the implementation of fundamental logic gates (NOT, NAND, and NOR), wherein two gate electrodes of all complementary transistor pairs are electrically connected. Furthermore, the gate-sharing structure eliminates the need for the fabrication of another layer of a gate electrode and shortens interconnect wiring paths.

As seen in Figure 1a, the 3D-COFET comprises nine vertically stacked functional layers, including two layers of OSCs, three layers of S/D and gate electrodes, two layers of gate dielectrics, and bottom/top encapsulation layers. First, a 1 μm thick parylene diX-SR film (KISCO, Ltd.) was deposited by chemical vapor deposition (CVD) on a glass substrate to provide a uniform and controlled surface condition for inkjet printing (Basement). Then, the S/D electrodes of the NFET were formed by printing Ag nanoparticle ink with a drop-on-demand piezoelectric inkjet printer (Fujifilm Dimatix, DMP-2831) (Metal 1). The structure was then treated with 4-methylbenzenethiol (4-MBT) to enhance the charge injection

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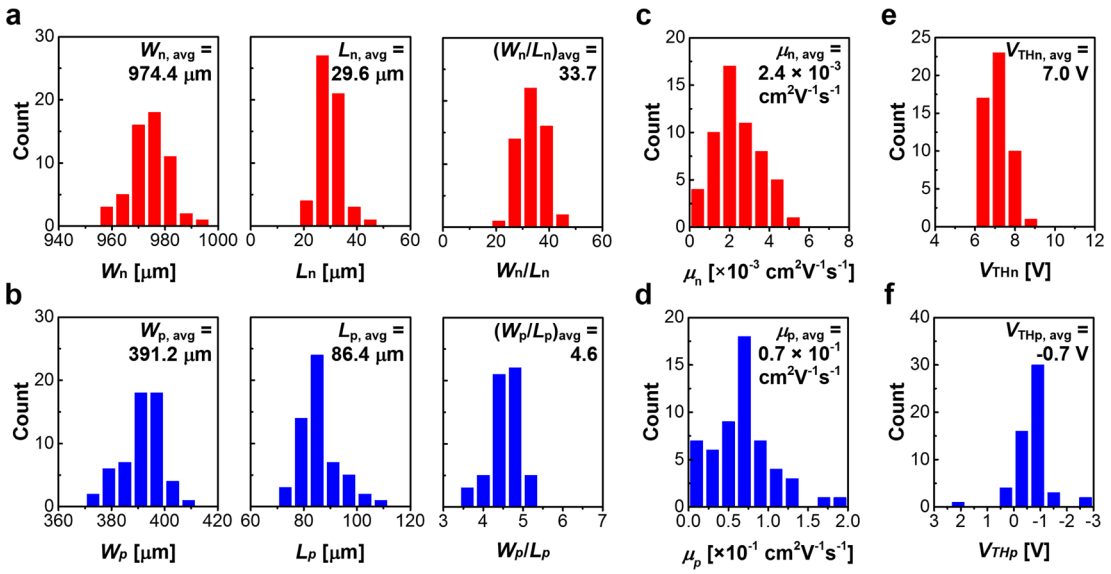

Figure 2. Histograms of (a,b) channel geometries (W and L), (c,d) carrier mobilities (μ), and (e,f) threshold voltages (V_{TH}) of 56 pairs of the NFETs (red) and the PFETs (blue) fabricated by inkjet printing.

between the S/D electrodes and the n-type active material.[28] An n-type polymer semiconductor, poly{[*N*,*N*′-bis(2-octyldodecyl)naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-*alt*-5,5′-(2,2′-bithiophene)} [P(NDI2OD-T2)] (0.3 wt %), dissolved in 1,2-dichlorobenzene was also inkjet-printed by the same printer to form a channel region between the S/D electrodes (N-type OSC). A parylene diX-SR film with a thickness of 230 nm was subsequently deposited as a gate dielectric of the NFET (Dielectric 1). A gate electrode was printed to finish the top-gate n-type device fabrication (Metal 2). In order to stack a PFET over the printed NFET, another dielectric layer of parylene diX-SR (440 nm) was deposited (Dielectric 2), on which S/D electrodes for the PFET were printed (Metal 3). The work function of the Ag electrodes was modified by treating with pentafluorobenzenethiol (PFBT) for efficient charge injection.[29] 2,8-Difluoro-5,11-bis-(triethylsilylethynyl)anthradithiophene (diF-TES-ADT; 2 wt %) blended with 0.5 wt % polystryrene in mesitylene was inkjet-printed between the S/D electrodes for the last step of the PFET fabrication (P-type OSC). The fabricated COFET device was passivated by a 1 μm thick parylene diX-SR film (Passivation). Finally, via-holes with sizes of 50 × 100 μm were formed on predefined locations by a nanosecond pulsed laser (V-Technology, VL-C30). The electrode lines of individual transistors on different floors were interconnected through these holes, as designed by the inkjet printing of Ag ink, to demonstrate the ICs (Metal 4).

Through this fabrication process, we printed an array of 3D-COFETs comprising 56 pairs (112 transistors in total) with pitches (the distances between two adjacent devices) of 3 and 2 mm in the x and y directions, respectively. Figure 1b shows an optical image of all 56 COFETs. A single COFET and its printed channels can be seen in Figure 1c,d, respectively. The two drain nodes of each 3D-COFET device were connected through a via-hole to form an inverter logic gate, which is the most fundamental building block of a digital IC.

Complementary transistor matching is very important in designing robust digital ICs. In particular, the drain current through a NFET should equal that through a PMOS for optimum operation in the complementary configuration. As can be seen in Figure 1e, the transfer characteristics of the printed NFET and PFET are measured at room temperature under ambient condition at V_{DS} = ±1 V for linear operation and ±20 V for saturation operation. Both devices showed well-matched performance with a maximum drain−source current I_{DS} of ∼0.3 μA at drain−source voltages V_{DS} of 20 and −20 V for both PFET and NFET. The matched I_{DS} was achieved by adjusting the dielectric layer thickness as well as the channel aspect ratios (W/L) of the NFET and PFET.[26] The dielectric layer of the NFET is about twice as thin as that of the PFET, and the W/L is about seven times as large. The NFET and PFET have a similar level of I_{DS} with on/off ratios of ∼10^5 and turn on at 2 and 0 V, respectively. The I_{DS}−V_{DS} curves with 2 V steps of gate−source voltage V_{GS} (Figure 1f) show the saturation behavior of I_{DS}, where I_{SD} is a negative expression of I_{DS} in the PFET. Under high contact resistance, the PFET is unsaturated in a wide range of V_{DS}.

Next, we examined the uniformity of the printed devices. Uniformity is an important issue in printed electronics. Inkjet printing is known to have a drop accuracy of ±5 μm due to variations in the flight trajectory of inkjet droplets and their spreading on the substrate surface.[5] Clearly, the positional deviation during printing affects the uniformity of the channel geometries among inkjet-printed S/D electrodes and the morphologies of the organic semiconducting films formed in the channels, which could lead to large variations in transistor performance. This increased transistor variability can pose a critical challenge when building complex computing circuits.

Remarkably, the fabrication yield reached 100% for the 56 COFETs (112 transistors) printed on a substrate. The uniformity of these devices was examined by measuring their properties, including channel geometry (W and L), saturation carrier mobility, and threshold voltage. Figure 2a−f shows the histograms of the statistical variation in W, L, the hole/electron mobilities (μ_n and μ_p), and threshold voltages (V_{THn} and V_{THp}), respectively. Most of the measured W and L values lie within ±10 μm of their mean values (Figure 2a). For the NFETs, the average W and L ($W_{n,avg}$ and $L_{n,avg}$) are 974.4 and 29.6 μm, respectively, with an average aspect ratio $(W_n/L_n)_{avg}$ of 33.7. Meanwhile, the average W and L of the PFETs ($W_{p,avg}$ and

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$L_{p,avg}$) are 391.2 and 29.6 μm, and the average aspect ratio $(W_p/L_p)_{avg}$ is 4.6 (Figure 2b). The W_p/L_p shows a wider distribution than W_n/L_n, implying a trade-off between reducing channel length and increasing uniformity in inkjet-printed transistors. The distributions of W/L exhibit variations of 14% for the NFETs and 8% for the PFETs. The values of μ_n and μ_p were extracted from the saturation I_{DS} (or I_{SD}) curves at V_{DS} = 20 V (or −20 V) using the drain saturation current equation with a dielectric constant of 4.1. All the transistors were measured immediately after fabrication. The n-type transistors have an average electron mobility ($\mu_{n,avg}$) of 2.4 × 10^{-3} cm^2 V^{-1} s^{-1} with a maximum value of 5.2 × 10^{-3} cm^2 V^{-1} s^{-1} (Figure 2c). In contrast, the stacked p-type transistors have an average hole mobility of 7 × 10^{-2} cm^2 V^{-1} s^{-1} with a maximum value of 0.2 cm^2 V^{-1} s^{-1} (Figure 2d). The respective extracted V_{THn} and V_{THp} values of the NFETs and PFETs are 7 and −0.7 V on average (Figure 2e,f), with small deviation.

The shelf-life stabilities of the inkjet-printed 3D-COFETs have been examined by measuring the transfer characteristics immediately after fabrication and again after 8 months. The devices were stored without additional encapsulation under ambient conditions (Supporting Information Figure S2). The transistor-on-transistor structure enhances the stability because of the multiple functional layers stacked on top of each other. In our device, the n-type OSC P(NDI2OD-T2) layer was passivated by three layers of parylene diX-SR (1.67 μm in total), while the p-type diF-TES-ADT layer was passivated by one parylene diX-SR layer (1 μm). The inkjet-printed NFET devices showed an average threshold voltage shift of ∼4 V, while there was no significant change in the average carrier mobility. The PFET transistors showed a ∼20% degradation in average carrier mobility and an average threshold voltage shift of ∼1 V. The on/off ratios of $|I_{DS}|$ of the complementary transistors were still higher than 10^4. We observed that both types of transistors exhibited positive shifts in the threshold voltages, probably due to the oxidation of OSCs.[30]

With the high yield, uniformity, and stability of the devices fabricated by the robust inkjet-printing process, we implemented 3D inverters using the 56 vertically stacked COFETs. The typical output curves of an inverter at operation voltages of VDD = 10 and 20 V are shown in Figure 3a. The maximum voltage gain (G_{MAX}) of the 56 inverters was 31.6 in dB scale on average, and most G_{MAX} values were within 25−35 dB, as seen in Figure 3b. The static noise margin (SNM), which indicates the immunity of logic gates to additive noise signals, was calculated by dividing the maximum length between the corners of the square inside the butterfly curve by VDD/2, as presented in Figure 3c. The measured SNMs of the 56 inverters were normally distributed, and their average was 45.8% with a standard deviation of 11.3% (Figure 3d). To further test the performances of the 3D inverters, 11 of them were connected in series to implement an 11-stage voltage-controlled ring oscillator, which is an important building block in digital and analogue circuits. To remove the loading effect of probing during the measurement, a five-stage inverting buffer was connected to the output node of the ring oscillator. Figure 3e shows the output voltage waveform of the ring oscillator at the operation voltage of 30 V. The oscillation frequency (f_{osc}) of the ring oscillator varied from ∼0.02 to ∼3 Hz when VDD was increased from 10 to 30 V, and the timing delay of the single inverter (the oscillation period divided by 22) decreased from 2.7 s to 14 ms, as shown in Figure 3f. The circuit design and detailed operation results can be found in Figure S3.

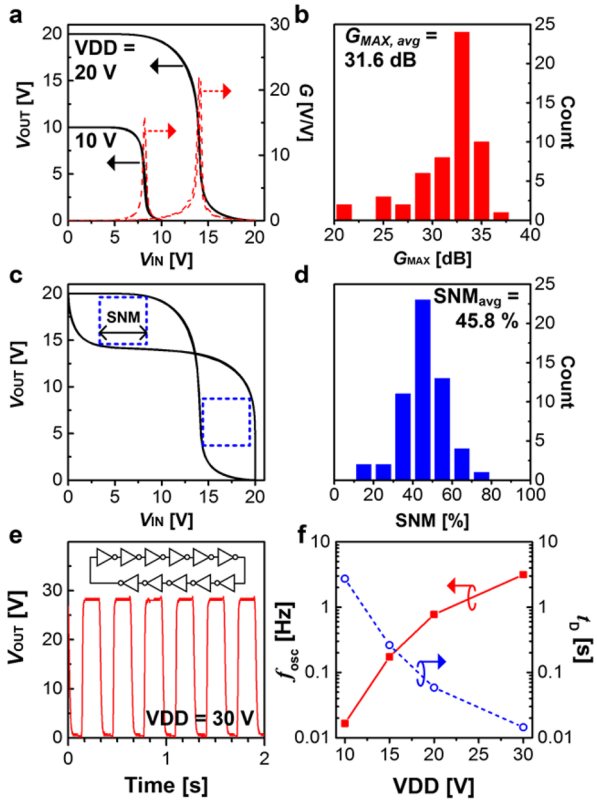

Figure 3. (a) Typical inverter output (solid line, left *y*-axis) and gain (dashed line, right *y*-axis) curves at VDD = 10 and 20 V. (b) Histogram of maximum voltage gains in dB scale of the 56 inverters with the average value of 31.6 dB. (c) Butterfly inverter curve for static noise margin (SNM) calculation at VDD = 20 V (the maximum length between the corners of the square divided by VDD/2). (d) SNM histogram of the 56 inverters. (e) Output voltage waveform of the 11-stage ring oscillator with operation voltage = 30 V. (f) Oscillation frequency (f_{osc}) of the ring oscillator and the timing delay of the single inverter (t_d) *vs* operation voltage (VDD).

Finally, we applied our printing process and the 3D transistor-on-transistor structure to fabricate a more complex computing device. First, we fabricated a universal NAND logic gate comprising two PFETs in parallel and two NFETs in series, as illustrated in Figure 4a. Next, a full adder, a basic computing unit of a microprocessor, was implemented by connecting nine NAND gates having 18 COFETs. Figure 4b,c shows the schematic circuit design of the full adder comprising nine NANDs and the actual demonstration of two inkjet-printed full adders, respectively. The circuit adds the binary inputs (A and B) and accounts for the carry-in (C_{IN}) to output the sum (S) and the carry-out (C_{OUT}); this addition operation can be extended to perform other fundamental arithmetic operations such as subtraction, multiplication, and division. The unit 3D NAND gates were designed to have a compact layout containing two 3D-COFETs with all their VDD and ground nodes commonly connected (Figure 4d). The four metal layers enabled the patterning of complex circuits with enhanced integration density of the routing lines and transistors. Figure 5a shows the representative DC characteristics at VDD = 20 V. The unit 3D NAND gives a robust logic value of "0" when both inputs are "1"; otherwise, it outputs "1". The inkjet-printed full adder was measured at the same VDD level. As shown in Figure 5b, the measurement results match exactly with the results of

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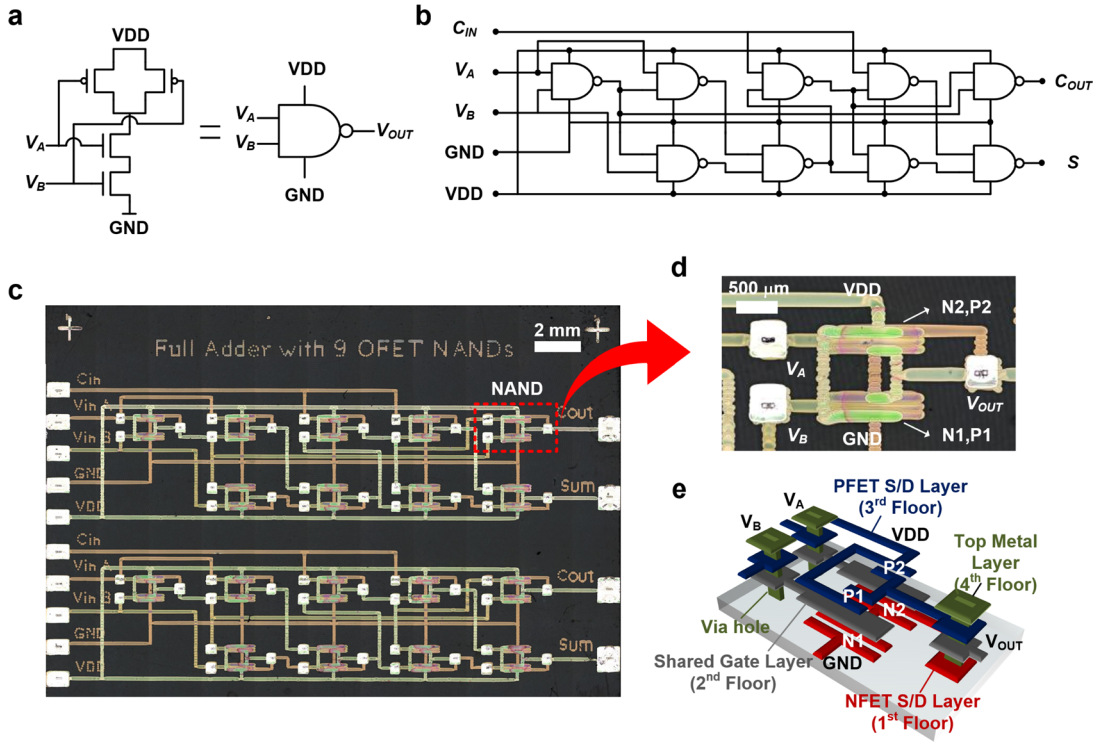

Figure 4. (a) Schematic circuit and symbol of a universal logic gate NAND. (b) Schematic circuit of a full adder with nine NAND gates. (c) Microscope image (top view) of an inkjet-printed organic 3D IC containing two full adders. (d) Magnified image and (e) 3D schematic metal routing plan of a single NAND gate comprising two 3D-COFETs.

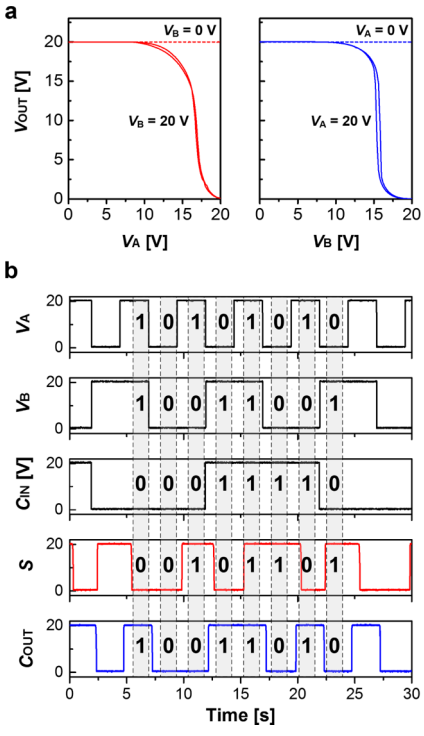

Figure 5. (a) DC output characteristics of a NAND gate with a fixed V_B (left) or V_A (right). (b) Input (V_A, V_B, and C_{IN}) and output (S and C_{OUT}) voltage waveforms of a full adder (binary numbers the indicate logic value of the state).

the full-adder Boolean equations ("$S = A \oplus B \oplus C_{IN}$", "$C_{OUT} = A{\cdot}B + C_{IN}{\cdot}(A \oplus B)$"). For example, when $A = B =$ "1" and $C_{IN} =$ "0", it gives $S =$ "0" and $C_{OUT} =$ "1".

The robustness and reliability of the 3D-COFETs have been well-demonstrated by the 3D design and fabrication of the full adder, which is a basic building block for a microprocessor. The major advantages of 3D transistor structure are as follows: (i) Increased transistor density. The effective size of the transistors is halved by stacking two transistors, and there is a potential to continue to reduce the size by vertically integrating more components in a unit area. The footprint of the 3D-COFET (excluding the areas of the four pads and the peripheral wires) is approximately 450 × 1000 μm (equivalent to approximately 0.23 mm^2 per transistor). The transistor density of the printed full-adder circuit is 0.41 transistors per mm^2, including the areas of the 3D transistors and all the routing wires. This value is several times higher than that of previously reported inkjet-printed organic circuits (~0.1 transistors per mm^2 for a ring oscillator[31] and ~0.06 transistors per mm^2 for a counter[32]). (ii) Efficient interconnection. The number of gates for complementary integrated circuits is halved thanks to the gate-shared structure of the 3D-COFETs. In addition, vertical interconnection through via-holes makes the circuit routing much simpler. The availability of multiple metal layers in the 3D structure (four layers were used in this work) allows more flexibility for interconnect routing, and as a result, the overall footprint occupied by interconnections is greatly reduced. (iii) Improved long-term stability. We showed that our 3D devices maintained their performances after 8 months of storage without additional encapsulation under ambient conditions. In our work, parylene was used as a dielectric because of a useful combination of electrical properties and a very low permeability to moisture and other corrosive gases. It is obvious that a NFET fabricated under a PFET is effectively protected by having several layers of parylene in terms of long-term stability. However, there still remains a challenge to develop a solution-

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processable polymer dielectric alternative to the CVD-processed dielectric for fully printed 3D transistor circuits.

CONCLUSION

In conclusion, we demonstrated a process for printing 3D-COFETs that can vertically stack different types of transistors. In the 3D-COFET structure, the bottom-gate PFET was fabricated directly on the top of the top-gate NFET, doubling the transistor density to 4.4 transistors per mm^2. This process has the potential to continue to stack transistors vertically and further increase transistor density. The inkjet-printed devices showed an exceptional yield of 100%, adequate noise margin (45.8%), and long-term stability of over 8 months. The robustness of our inkjet-printing process for the fabrication of 3D digital circuits was examined by evaluating the parameters (*e.g.*, carrier mobility, threshold voltage, channel geometry, gain, and SNM) of all the printed devices on a substrate. With the 3D transistor-on-transistor structure and robust inkjet process, we implemented several digital circuits, including an array of inverters, a ring oscillator, and a full adder. The successful fabrication of a full adder, an important arithmetic logic circuit, by printing is of paramount importance for the realization of a fully printed flexible and wearable computing system. Our 3D inkjet-printing approach provides a path for achieving high transistor density, high yield, high uniformity, and long-term stability, which are critical for the realization of organic digital ICs and other intelligent devices.

MATERIALS AND METHODS

Device Fabrication. The Ag nanoparticles (55 wt %, Harima, NPS-JL) were prepared and dissolved in tetradecane as a conductive metal ink. For the n-type organic semiconductor ink, P(NDI2OD-T2) (0.3 wt %) was dissolved in 1,2-dichlorobenzene and stirred at 70 °C. For the p-type semiconductor ink, diF-TES-ADT (2 wt %) and polystyrene (0.5 wt %, average M_w = 280 000 g mol^{-1}, Sigma-Aldrich) were codissolved in mesitylene and stirred at room temperature. The semiconductor inks were filtered with a 0.45 μm PTFE filter and then used to fill ink cartridges. On a glass substrate (Corning, Eagle XG), a parylene diX-SR layer (thickness ≈ 1 μm) was deposited by CVD for the basement layer and then annealed at 120 °C for 30 min in a nitrogen-filled glovebox. The NFET Ag S/D electrodes were printed using an inkjet printer (Fujifilm Dimatix, DMP2831) in an ambient environment and then sintered at 120 °C for 30 min in the glovebox. The NFET S/D electrodes were dipped into a 4-MBT solution [(10 mM in isopropyl alcohol (IPA)] for 5 min and then rinsed with IPA. The n-type ink was inkjet-printed between the Ag S/D electrodes and then annealed at 120 °C for 10 h. A dielectric layer of parylene diX-SR was deposited (thickness ≈ 230 nm). Next, the Ag gate electrode was printed and then sintered at 120 °C for 30 min in an inert atmosphere. The PFET dielectric layer was deposited (thickness ≈ 440 nm). The PFET S/D electrodes were printed on the film and then annealed at 120 °C for 30 min in an inert glovebox. The PFET S/D electrodes were dipped in a PFBT solution (30 mM in IPA) for 5 min and then rinsed with IPA. The diF-TES-ADT was printed in the channel region, and the sample was dried at 80 °C for 30 min. The device was encapsulated with the parylene diX-SR. The interconnection via-holes were formed by a nanopulse laser (V-Technology, VL-C30), and the holes were then filled with the printed Ag.

Inkjet-Printing Process. All the metal electrodes and organic semiconductors were inkjet-printed using a piezo-actuated inkjet nozzle generating small drops with a volume of ~10 pL. For printing of the Ag ink, the temperatures of a nozzle and a substrate were set to 35 and 53 °C, respectively, for stable and reliable printing. The temperatures for OSC printing were set to 30 °C. The drop spacing was 60, 20, and 5 μm for patterning the metal, the n-type OSC, and the p-type OSC inks, respectively. Detailed information about the printed Ag line profile and morphology can be found in our previous report.[27,33]

Performance Measurements. The DC characteristics of the 3D-COFETs, the inverters, and the NAND gate were measured using a semiconductor parameter analyzer (Keithley, 4200-SCS) under the ambient conditions. The output waveforms of the ring oscillator with a five-stage voltage buffer were acquired by an oscilloscope (Tektronix, DPO2024B). For the measurement of the full adder, the input pulse signals were generated by function generators (Agilent, 33522A) and then amplified by amplifiers (Agilent, 330502a) to achieve amplitudes of 20 V. The output waveforms were acquired by the oscilloscope. Because the output currents of the full adder were not sufficient to drive the input impedance of the oscilloscope probe, commercial voltage buffer ICs (Texas Instruments, CD4050E) were connected to the output nodes and the oscilloscope input ports. The measurement setup is shown in Figure S1 of the Supporting Information.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.6b06041.

Experimental setup for printed ICs; long-term stability of the 3D-COFETs; characteristics of a ring oscillator; layouts for the ring oscillator and full adder (PDF)

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Notes

The authors declare no competing financial interest.

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